CSIR-UGC-NET/JRF | GATE

TIFR|BARC|JEST|IISc|DRDO|ISRO|SLET|ONGC-GT & Ph.D. Entrance

Assignment

Electronics

PHYSICAL SCIENCES

CAREER ENDEAVOUR
ACADEMY PRIVATE LIMITED

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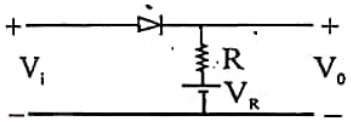
Assignment : Network

1. For the given clipper-circuit shown in figure. If V_i is the input voltage and V_o is the output voltage.



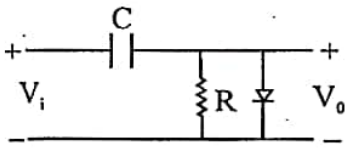
(a) the circuit clipps off the input for $V_i < V_R$

(b) The circuit clipps off the input for $V_i > V_R$

(c) The negative swings of V_i are only clipped off

(d) The output $V_0 = V_R$ always.

2. Which statements are true about give ckt.



(a). It is clipper (b) It is rectifier

(c) It is a clamping circuit that would clamp positive peaks to near zero.

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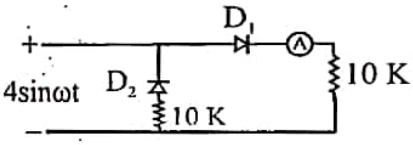
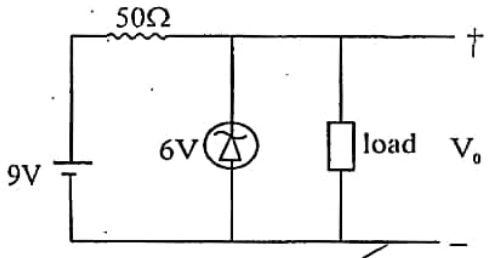
3. In circuit of given figure assume that diodes are ideal and meter is an average indicating ammeter then ammeter will read.



(a) $0.4\sqrt{2}$ mA (b) 0.4 mA (c) $\frac{0.8}{\pi}$ mA (d) $\frac{0.4}{\pi}$ mA

4. A Zener-diode shown in figure has a knee current of 5 mA and a maximum allowed power dissipation of 300 mw. What are the minimum and maximum load currents that can be drawn safely from circuit, keeping the output voltage constant at 6 volt



(a). 0 mA, 180 mA (b) 5 mA, 110 mA (c) 10 mA, 55 mA (d) 60 mA, 180 mA

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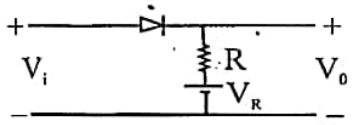

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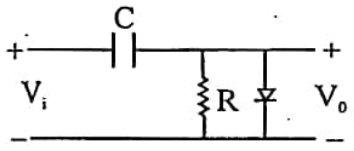

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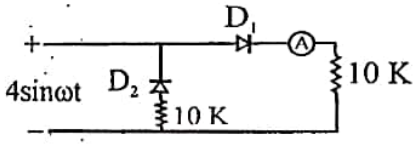

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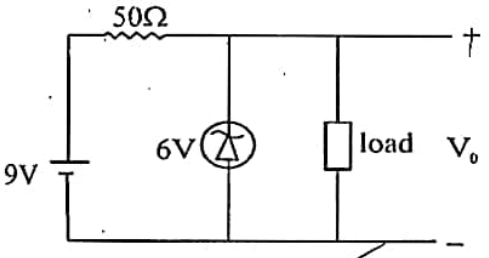

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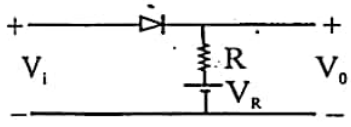

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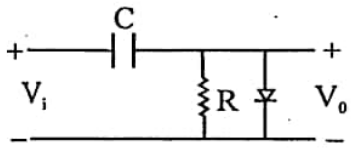

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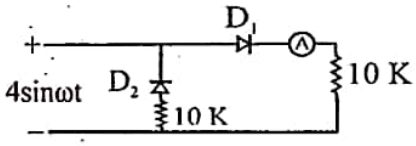

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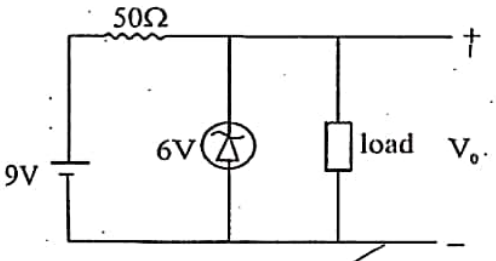

(a). 0 mA, 180 mA (b) 5 mA, 110 mA (c) 10 mA, 55 mA (d) 60 mA, 180 mA

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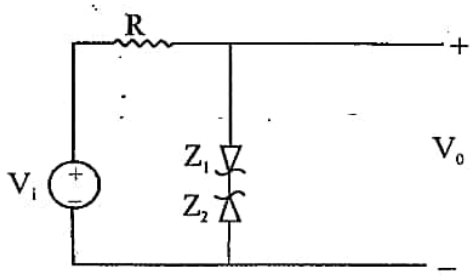
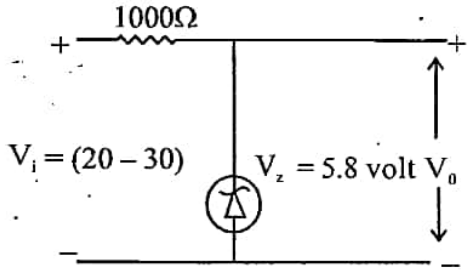
5. In the circuit-shown in figure, zener voltage $V_{z_1} = V_{z_2} = 4.0$ volt, cut-involtage of diode = 0.7 volt



(a) If $|V_i| < 4.7V$, then $V_0 = V_i$ (b) If $|V_i| < 8V$, then $V_0 = V_i$

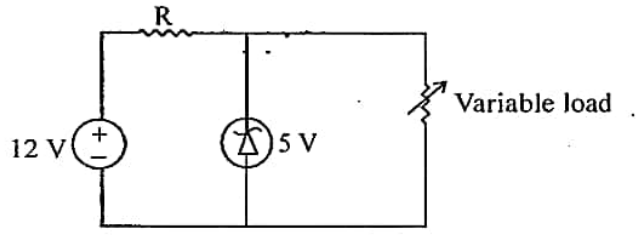
(c) If $|V_i| > 4.7$ V, then $V_0 = V_i$ (d) $V_0 = 4.7$ volt for all values of V_i

6. The zener-diode in regulator circuit shown in figure. has a zener-voltage of 5.8 volt and a zener knee current of 0.5 mA, then maximum load current drawn from circuit, ensuring proper functioning over, input voltage range b/w (20-30) volt is:



(a) 23.7 mA (b) 14.2 mA (c) 13.7 mA (d) 24.2 mA

7. In the voltage regulator shown in figure, the load current can vary from (100-500) mA, assuming that zener-diode is ideal (i.e. zener knee current is negligible & small, here zever resistance is zero in break-down region) Then what is the value of R?



(a) 7Ω (b) 70Ω (c) 70 / 3Ω (d) 14Ω

8. The resistivity at room temperature of intrinsic Si is $2.3 \times 10^3\ \Omega - m$ and that of an extrinsic N- type Si, sample is $8.33 \times 10^{-2}\ \Omega -$ met. A bar of this extrinsic Si, sample is 3 mm long and has a rectangular cross-section 50×100 mm and a steady state current of 1μA exists in the bar, if voltage across the bar is found to be 50 mv. If same bar is of intrinsic Si, then voltage across bar will be about.

(a). 1400 volt (b) 140 volt (c) 14 volt (d) 1.4 volt

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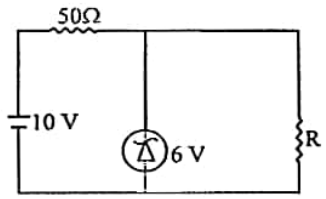
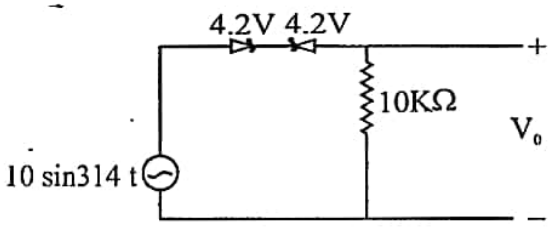
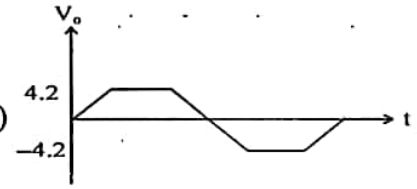
9. The 6V, Zener-diode shown in figure has zero zener resistance and a knee current of 5mA. The minimum value of R, so that voltage across it does not fall below 6 V is:

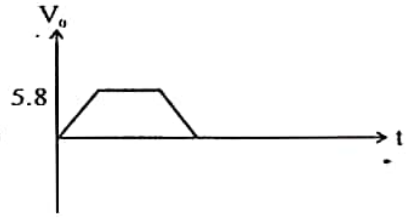


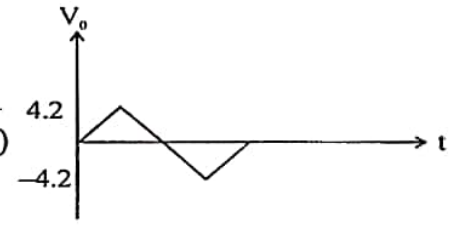
(a) 1.2kΩ (b) 80Ω (c) 50Ω (d) 0Ω

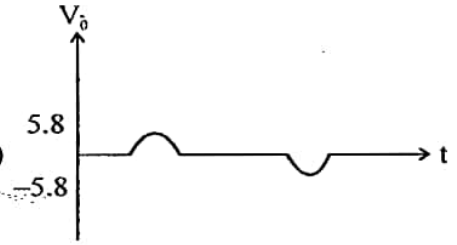
10. Draw wave shape V_0 for the given figure.



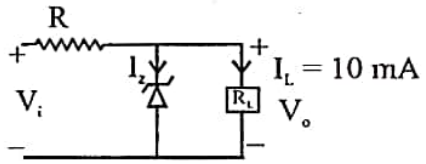
(a)


(b)


(c)


(d)


11. A zener-diode regulator shown in figure is to be designed to meet the specifications: $I_L = 10mA$, $V_0 = 10volt$ and V_{in} varies from 30-50V if zener-diode has $V_z = 10$ volt & $I_{zk} = 1$ mA then for satisfactory operation



(a) $R \leq 1800\Omega$ (b) $1800\Omega \leq R 3600\Omega$ (c) $3700\Omega \leq R \leq 4000\Omega$ (d) $R > 4000\Omega$

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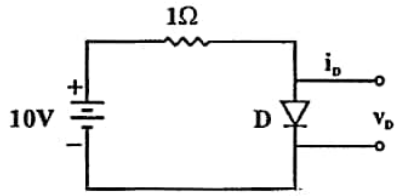
12. A diode D as shown in the circuit as an i–v relation which can be proximated by

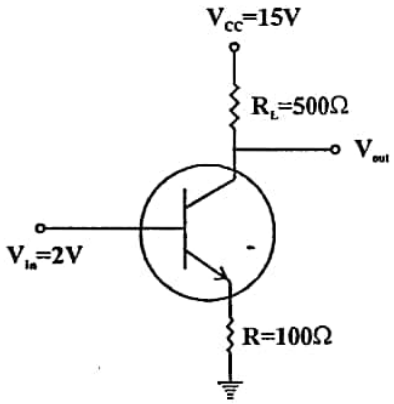
$$i_D = \begin{cases} v_D^2 + 2v_D, & \text{for } v_D > 0 \\ 0, & \text{for } v_D \le 0 \end{cases}$$



The value of v_D in the circuit is:

(a) $\left(-1+\sqrt{11}\right)$V (b) 8V (c) 5V (d) 2V

13. The circuit depicted on the right has been made with a silicon n-p-n transistor. Assuming that there will be a 0.7V drop across a forward-biased silicon p-n junction, the power dissipated across the transistor will be, approximately,



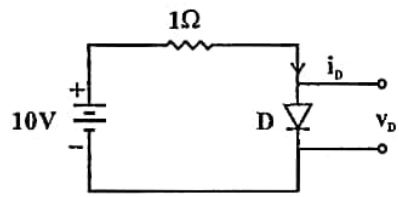
(a) 53 mW (b) 94 mW (c) 17 mW (d) 67 mW

14. A live music broadcast consists of a radio-wave of frequency 7 MHz, amplitude-modulated by a microphone output consisting of signals with a maximum frequency of 10 KHz. The spectrum of modulated output will be zero outside the frequency band

(a) 7.00 MHz to 7.01 MHz (b) 6.99 MHz to 7.01 MHz
(c) 6.99 MHz to 7.00 MHz (d) 6.995 MHz to 7.005 MHz

15. A diode D as shown in the circuit as an i–v relation which can be proximated by

$$i_D = \begin{cases} v_D^2 + 2v_D, & \text{for } v_D > 0 \\ 0, & \text{for } v_D \le 0 \end{cases}$$



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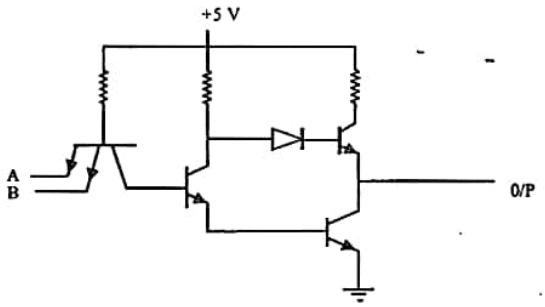
Data for linked Q.16 and Q.17.

In the I.C. logic gate, shown in figure. If thresold voltage V_{BE} is 0.75 volt and V_{CE} (sat) = 0.2 V, calculate value of output voltage.



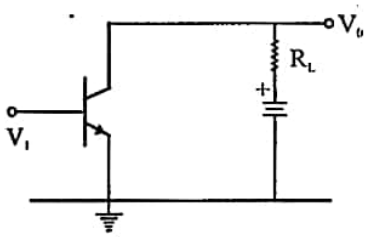
16. If $V_A = V_B = 4.5$ volt

(a) 0.75 V (b) 0.55 V (c) 5V (d) 0.2 V

17. If $V_A = 4.5$ volt, $V_B = 0.2$ volt

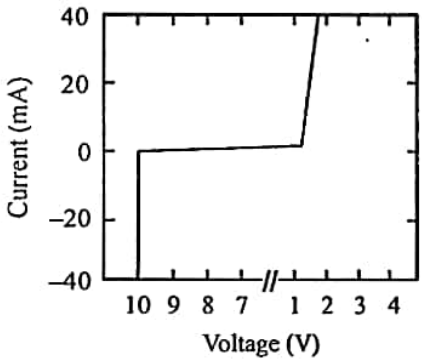
(a) 0.75 V (b) 0.55 V (c) 5V (d) 0.2 V

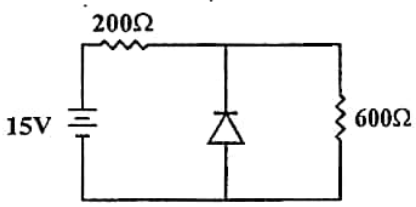
18. The transistor in the given circuit has $h_{fe} = 35\Omega$ and $h_{ie} = 1000\Omega$. If the load resistance $R_L = 1000\Omega$, the voltage and current gain are, respectively.



(a) –35, +35 (b) 35, 35 (c) 35, 0.97 (d) 0.98, 35

19. The figure on the right shows the current-voltage characteristics of a diode over a range of voltage and current where it is safe to operate the diode.





When this diode is used in the circuit on the extreme right, the approximate current, in mA, through the diode will be

(a) 0 (b) 8.3 (c) 16.7 (d) 25

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20. Match the following:

(a) Hartley	(b) Wien bridge	(c) Crystal
1. Low frequency oscillator		2. High frequency oscillator
3. Stable frequency oscillator		4. Relaxation oscillator
5. Negative resistance oscillator.		

(a) a-2 b-1 c-3 (b) a-1 b-2 c-3 (c) a-3 b-1 c-2 (d) a-5 b-4 c-1

21. In a common emitter BJT amplifier, the maximum usable supply voltage is limited by:
(a) Avalanche breakdown of Base-Emitter junction
(b) Collector-Base breakdown voltage with emitter open (BV_{CBO}).
(c) Collector-Emitter breakdown voltage with base open (BV_{CBO})
(d) Zener breakdown voltage of the Emitter-Base junction.

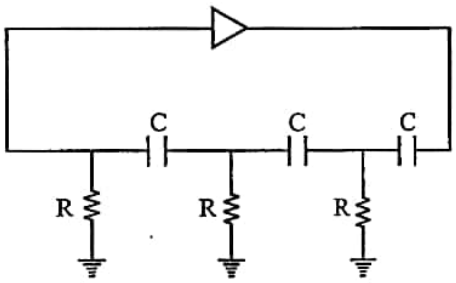
22. Choose the correct match for the input resistance of various amplifier configurations shown below:

Configuration	**Input resistance**
CB: Common Base	LO: Low
CC: Common Collector	MO: Moderate
CE: Common Emitter	HI: High

(a) CB-LO, CC-MO, CE-HI (b) CB-LO, CC-HI, CE-MO
(c) CB-MO, CC-HI, CE-LO (d) CB-HI, CC-LO, CE-MO

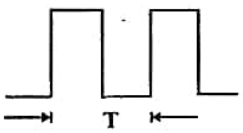
23. The cascode amplifier is a multistage configuration of:
(a) CC-CB (b) CE-CB (c) CB-CC (d) CE-CC

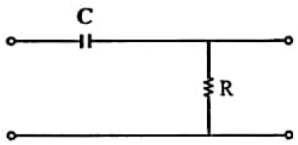
24. The oscillator circuit shown in figure has an ideal inverting amplifier. Its frequency of oscillation (in Hz) is:



(a) $\frac{1}{\left(2\pi\sqrt{6}\,RC\right)}$ (b) $\frac{1}{\left(2\pi\,RC\right)}$ (c) $\frac{1}{\left(\sqrt{6}\,RC\right)}$ (d) $\frac{1}{\sqrt{6}\left(2\pi\,RC\right)}$

25. For the circuit given in the figure, consider the following statements:
1. The output V_0 will consist of a positive and a negative spike if $RC << T$.
2. The output V_0 will be similar to v_1 if $RC >> T$.
3. The output will have a higher rise time if RC is made progressively smaller than T. Of these statements:





(a) 1, 2 and 3 are correct (b) 1 and 2 are correct
(c) 2 and 3 are correct (d) 1 and 3 are correct.

26. An ideal power supply has
(a) Zero internal resistance (b) Very large input resistance
(c) Very small output resistance (d) Very large output resistance

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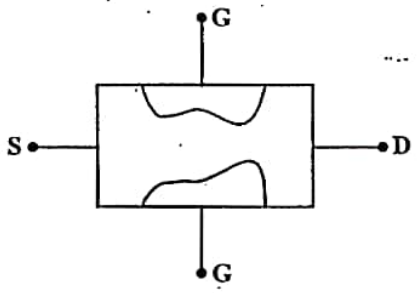
27. If $\alpha = 0.995$, $I_E = 10$ mA and $I_{CBO} = 0.5$ mA, then I_{CEO} will be

(a) 100 mA (b) 25 μA (c) 10.1 mA (d) 105 mA

28. The ripple factor of a power supply is given by (Symbols have the usual meaning)

(a) $\frac{P_{dc}}{P_{OC}}$ (b) $\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$ (c) $\sqrt{\left(\frac{I_{dc}}{I_{rms}}\right)^2 - 1}$ (d) $\frac{I_{dc}}{I_{rms}}$

29. In a biased JFET, the shape of the channel is as shown in the given figure because

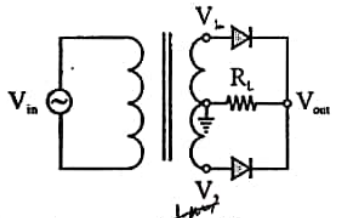


(a) It is the property of the material used
(b) The drain end is more reverse biased than source end
(c) The drain end is more forward biased than source end
(d) The impurity profile varies with the distance from source.

30. A Hartley oscillator is used for generation.

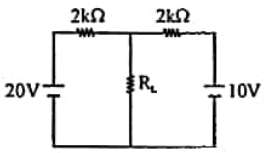
(a) Very low frequency oscillation (b) Radio frequency oscillation (High freq)
(c) Microwave oscillation (d) Audio-frequency oscillation.

31. For the rectifier circuit shown in the figure, the sinusoidal voltage (V_1 or V_2) at the output of the transformer has a maximum value of 10V. The load resistance R_L is 1 kΩ. If I_{av} is the average current through the resistor R_L the circuit corresponds to a.



(a) Full wave rectifier with $I_{av} = 20/\pi$ mA (b) Half wave rectifier with $I_{av} = 20/\pi$ mA
(c) Half wave rectifier with $I_{av} = 10/\pi$ mA (d) Full wave rectifier with $I_{av} = 10/\pi$ mA

32. In the circuit shown in the figure the Thevenin voltage V_{Th} and Thevenin resistance R_{Th} as seen by the load resistance R_L (=1kΩ) are respectively.



(a) 15V, 1 kΩ (b) 30 V, 4 kΩ
(c) 20 V, 2 kΩ (d) 10V, 5 kΩ.

33. The high input impedance of field effect transistor (FET) amplifier is due to

(a) The pinch-off voltage (b) Its very low gate current.
(c) The source and drain being far apart (d) The geometry of the FET.

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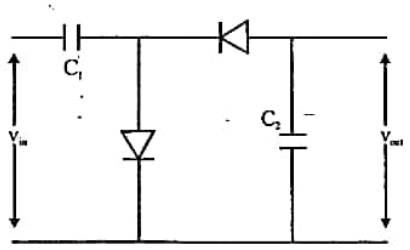
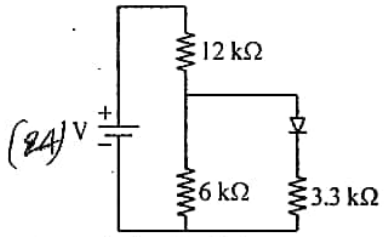
34. A sinusidal input voltage v_{in} of frequency ω is fed to the circuit shown in the figure, where $C_1 >> C_2$. If v_{in} is the peak value of the input voltage, then output voltage (v_{out}) is:



(a) $2v_{in}$ (b) $2v_0 \sin \omega t$ (c) $\sqrt{2}v_{in}$ (d) $\frac{v_{in}}{2} \sin \omega t$

35. In the following circuit, the voltage drop across the ideal diode in forward bias condition is 0.7V.



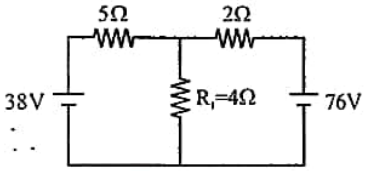
The current passing through the diode is

(a) 0.5 mA (b) 1.0 mA (c) 1.5 mA (d) 2.0 mA

36. In a typical n-p-n transistor the doping concentration in emitter, base and collector regions are C_E, C_B and C_C respectively. These satisfy the relation,

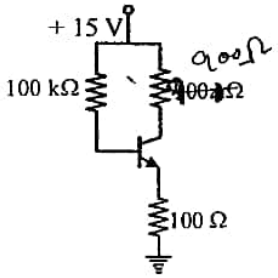
(a) $C_E > C_C > C_B$ (b) $C_E > C_B > C_C$ (c) $C_C > C_B > C_E$ (d) $C_E = C_C > C_B$

37. For the circuit shown, the potential difference (in Volts) across R_L is:



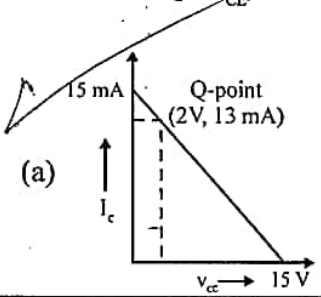
(a) 48 (b) 52 (c) 56 (d) 65

38. Consider the following circuit in which the current gain β_{dc} of the transistor is 100.

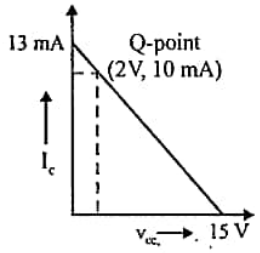


Which one of the following correctly represents the load line (collector current I_c with respect to collectr-emitter voltage V_{CE}) and Q-point of this circuit?

(a)



(b)



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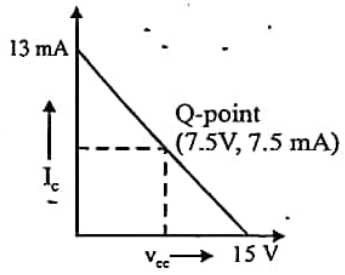
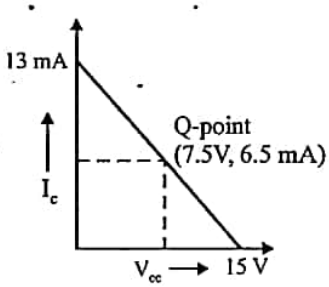
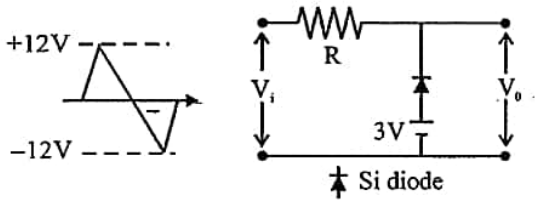
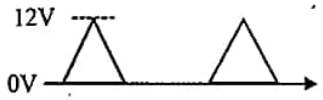
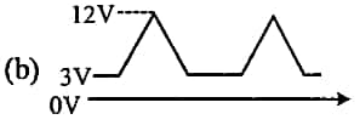
(c)


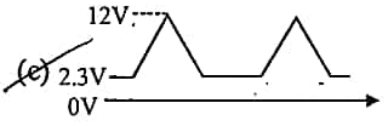
(d)


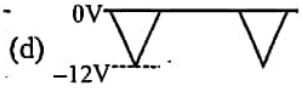
39. When an input voltage V_i, of the form shown, is applied to the circuit given below, the output voltage V_0 is of the form.



(a)


(b)


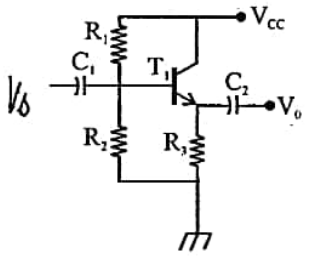
(c)


(d)


40. A common emitter transistor amplifier circuit is operated under a fixed bias. In this circuit, the operating point
(a) Remains fixed with an increase in temperature
(b) Moves towards cut-off region with an increase in temperature.
(c) Moves towards the saturation region with a decrease in temperature.
(d) Moves towards the saturation region with an increase in temperature

41. Under normal operating conditions, the gate terminal of an n-channel junction field effect transistor (JFET) and an n-channel metal oxide semiconductor field effect transistor (MOSFET) are
(a) Both biased with positive potentials.
(b) Both biased with negative potentials.
(c) Biased with positive and negative potentials, respectively.
(d) Biased with negative and positive potentials, respectively.

42. The circuit shown below



(a) Is a common-emitter amplifier
(b) Uses a pnp transistor
(c) Is an oscillator (with out i/p)
(d) Has a voltage gain less than one.

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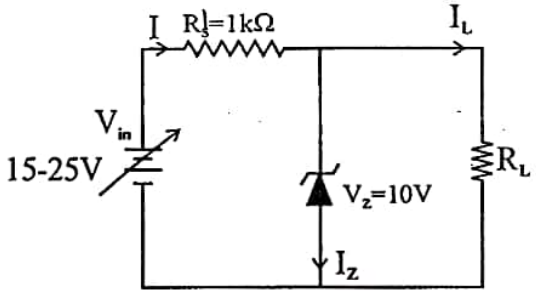
43. An amplifier of gain 1000 is made into a feedback amplifier by feeding 9.9% of its output voltage in series with the input opposing. If $f_L = 20$ Hz and $f_H = 200$ kHz for the amplifier without feedback, then due to the feedback.
(a) The gain decreasse by 10 times
(b) The outputresistance increases by 10 times
(c) The f_H increases by 100 times
(d) The input resistance decreases by 100 times.

44. Pick the correct statement based on the below circuit.



(a) The maximum Zener current, $I_{Z(max)}$, when $R_L = 10k\Omega$ is 15mA
(b) The maximum Zener current, $I_{z(min)}$, when $R_L = 10k\Omega$ is 5mA
(c) With $V_{in} = 20V$, $I_L = I_Z$, when $R_L = 2k\Omega$
(d) The power dissipated across the Zener when $R_L = 10k\Omega$ and $V_{in} = 20V$ is 100 mW.

45. A current amplifier is characterised by
(a) low input impedance and high output impedance
(b) high input impedance and low output impedance.
(c) low impedance at both input and output terminals.
(d) high impedance at both input and output terminals.

46. Which of the following characteristics DOES NOT belong to a common collector transistor amplifer?
(a) Low voltage gain [≈]
(b) High current gain.
(c) High input impedance
(d) High output impedance.

47. An amplifier has a voltage gain of 500 and an input impedance 20 KΩ, without any feedback. Now a negative feedback with $\beta = 0.1$ is applied. Its gain and input impedance with feedback will respectively be
(a) 9.8 and 392 K ohms
(b) 9.8 and 1020 K ohms
(c) 50 and 1020 K ohms
(d) 50 and 2 K ohms

48. A bipolar junction transistor used in common collector configuration has
(a) High input impedance and high output impedance
(b) High input impedance and low output impedance.
(c) Low input impedance and high output impedance.
(d) Low input impedance and low output impedance.

49. A transistor is said to be in saturation region when
(a) Both collector and emitter junctions are forward biased.
(b) Both collector and emitter junctions are reverse biased.
(c) The collector junction is forward biased but the emitter junction is reverse biased.
(d) The collector junction is reverse biased but the emitter junction is forward biased.

50. A zener diode is used as a voltage regulator across an unregulated DC source. Overloading will damage
(a) DC source only (b) Zener diode only (c) Both (a) and (b) (d) Neither (a) nor (b)

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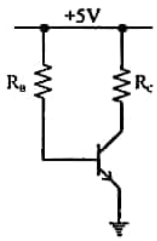
51. Which of the following are true for a field effect transistor (FET)?
(a) A FET has a very high power gain.
(b) A FET has a negative temperature coefficient of resistance.
(c) A FET has a very high input impedance.
(d) A FET is a current controlled device.

52. In the circuit on the right, $R_B = 1\ k\Omega$ and $R_C = 100\Omega$. If the transistor $\beta(h_{FE})$ is 100, the current through R_C will be



(a) ≈ 0.43 A
(b) ≈ 50 mA
(c) zero
(d) Oscillating between 0 and 50 mA.

53. In an n-p-n transistor, the leakage current consists of
(a) Electrons moving from the base to the emitter
(b) Electrons moving from the collector to the base
(c) Electrons moving from the collector to the emitter.
(d) Electrons moving from the base to the collector.

54. A piece of semiconducting material is introduced into a circuit. If the temperature of the material is raised, the circuit current will
(a) Increase (b) Remain the same (c) Decrease (d) Cease to flow.

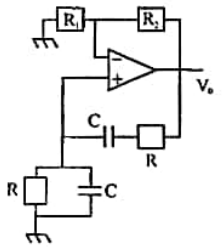
55. An n-channel silicon (dielectric constant = 12) FET with a channel width $a = 2\times10^{-6}$ m is doped with 10^{21} electrons/m^3. The pinch-off voltge is:
(a) 0.86 V (b) 0.68 V (c) 8.6 V (d) 6.8 V

56. An avalanche effect is observed in a diode when
(a) The forward voltage is less than the breakdown voltage.
(b) The forward voltage exceeds the breakdown voltage.
(c) The reverse voltage exceeds the breakdown voltage.
(d) The diode is heavily doped and forward biased.

57. A bipolar junction transistor with one junction forward biased and either the collector or emitter open, operates in the
(a) cut-off region (b) saturation region (c) pinch-off region (d) active region

58. A field effect transistor is a
(a) Unipolar device
(b) Special type of bipolar junction transistor.
(c) Unijunction device
(d) Device with low input impedance

59. What should be the values of the components R and R_2 such that the frequency of the Wien Bride oscillator is 300 Hz? [Given: $C = 0.01\ \mu F$ and $R_1 = 12\ k\Omega$]



(a) $R = 48k\Omega$ and $R_2 = 12k\Omega$
(b) $R = 26k\Omega$ and $R_2 = 24k\Omega$
(c) $R = 530\ k\Omega$ and $R_2 = 1\ M\Omega$
(d) $R = 53k\Omega$ and $R_2 = 24k\Omega$

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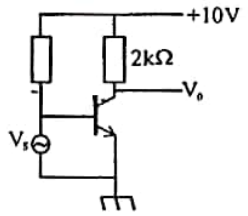
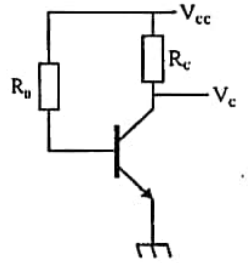
60. Figure shows a common emitter amplifier with $\beta = 100$. What is the maximum peak to peak input 500 kΩ signal (v_s) for which is distortion-free output may be obtained? [Assume $V_{BE} = 0$ and $r_e = 20\,\Omega$].



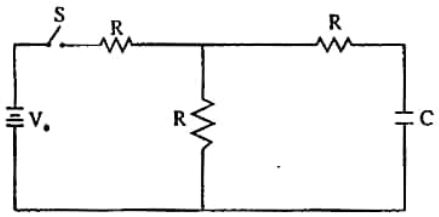
(a) 40 mV (b) 60 mV (c) 80 mV (d) 100 mV

61. Calculate the collector voltage (v_c) of the transistor circuit shown in the figure
[Given: $\alpha = 0.96$, $I_{CBO} = 20\mu A$, $V_{BE} = 0.3V$, $R_B = 100k\Omega$, $V_{CC} = +10V$ and $R_C = 2.2k\Omega$]



(a) 3.78 V (b) 3.82 V (c) 4.72 V (d) 9.7 V

62. A capacitor C is connected to a battery V_0 through three equal resistors R and a switch S as shown above: The capacitor is initially uncharged. At time t = 0, the switch S is closed. The voltage across the capacitor as a function of time t for t > 0 is given by

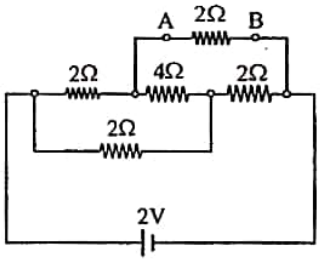


(a) $(V_0/2)(1-\exp(-t/2RC))$ (b) $(V_0/3)(1-\exp(-t/3RC))$

(c) $(V_0/3)(1-\exp(-3t/2RC))$ (d) $(V_0/2)(1-\exp(-2t/3RC))$

63. A junction field effect transistor behaves as a
(a) Voltage controlled current source (b) Voltage controlled voltage source
(c) Current controlled voltage source (d) Current controlled current source

64. For the circuit shown, the current passing through the 2Ω resistor (AB) is:



(a) 0.2 A (b) 0.5 A (c) 1.0 A (d) 2.0 A

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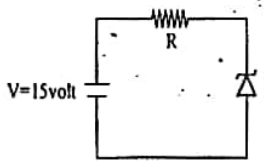
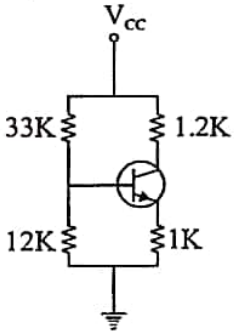
65. The Zener diode in the following circuit has a power rating of 100 mw and the Zener break down voltage is. 10 volt. If the input supply voltage is 15 V dc, the minimum value of resistance R, in ohms, should be

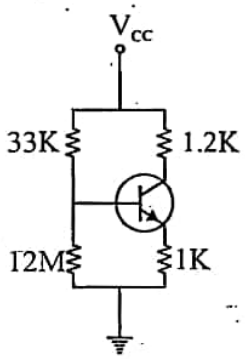


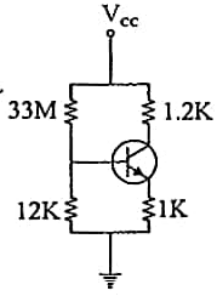
(a) 100 (b) 150 (c) 250 (d) 500

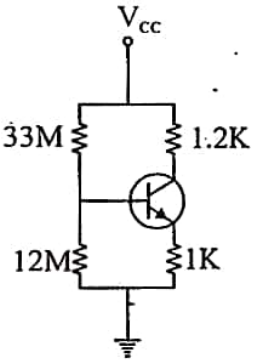
66. Transistor is acts as a switch in region
(a) Cut off (b) Saturation (c) Active region (d) None of these

67. Which of the following circuits has an appropriate voltage divider for biasing the transistor?

(a)


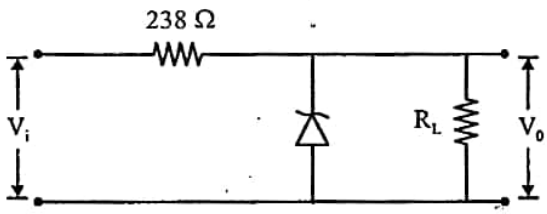
(b)


(c)


(d)


68. Which of the following statements is correct for a common emitter amplifier circuit?
(a) The output is taken from the emitter
(b) There is 180° phase shift between input and output voltages
(c) There is no phase shift between input and output voltages
(d) Both p-n juntions are forward biased.

69. The voltage regulator circuit shown in the figure has been made with a Zener diode rated at 15V, 200 mW. It is required that the circuit should dissipate 150 mW power across the fixed load resistor R_L



For stable operation of this circuit, the input voltage V_i must have a range
(a) 17.5 V, 20.5 V (b) 15.5 V, -20.5 V
(c) 15.5 V, -22.5 V (d) 17.5 V, -22.5 V

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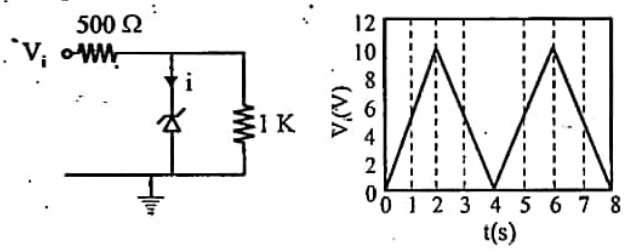
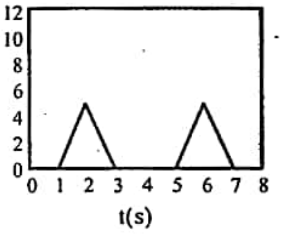
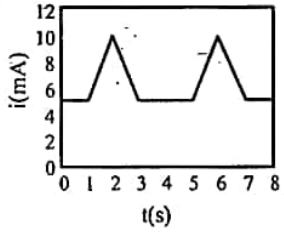
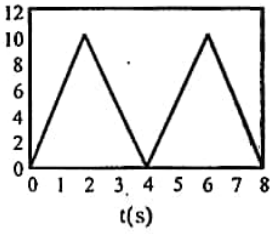
70. The figure below shows a voltage regulator utilizing a Zener diode of breakdown voltage 5V and a positive triangular wave input of amplitude 10V.

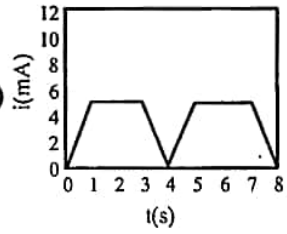


For $V_i > 5V$, the Zener regulates the output voltage by channeling the excess current through it self. Which of the following waveforms shows the current 'i' passing through the Zener diode?

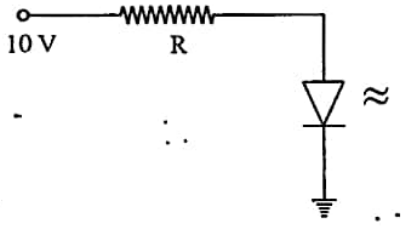
(a) 

(b) 

(c) 

(d) 

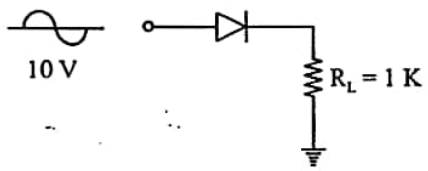
71. A red LED is used as a power indicator in an instrument powered by a 10V dc source. The appropriate value of the resistance R in the indicator bias circuit shown below is optimum current for LED 10mA

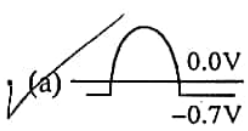


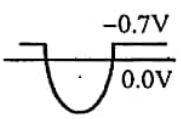
(a) 20 kΩ (b) 1 kΩ (c) 200 kΩ (d) 100 Ω

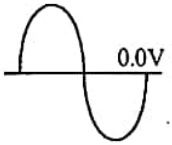
72. For operation as an amplifier, the base of an n-p-n transistor must be
(a) negative with respect to the emitter (b) positive with respect to the emitter
(c) positive with respect to the collector (d) at zero volt

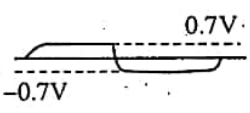
73. A sinusoidal voltage of amplitude 10V drives the following circuit. If the voltage across R_L is viewed on an oscilloscope, which one of the representative waveforms you would expect to see?



(a) 

(b) 

(c) 

(d) 

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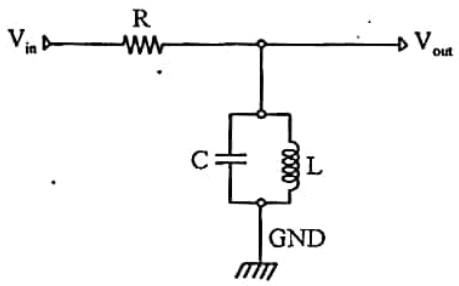
74. The circuit



describes a

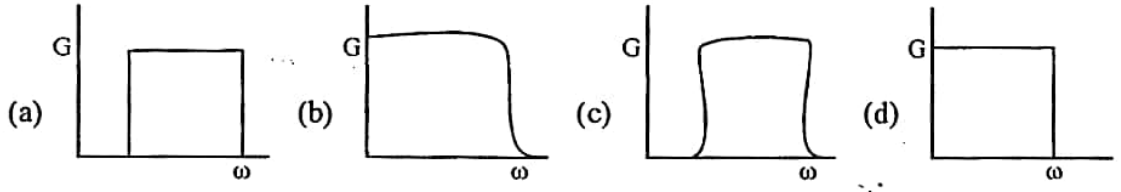
(a) band reject filter rejecting frequencies near $f = \frac{1}{2\pi\sqrt{LC}}$

(b) band pass filter allowing frequencies near $f = \frac{1}{2\pi\sqrt{LC}}$

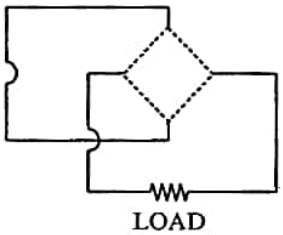
(c) high pass filter allowing $f > \frac{1}{2\pi\sqrt{LC}}$

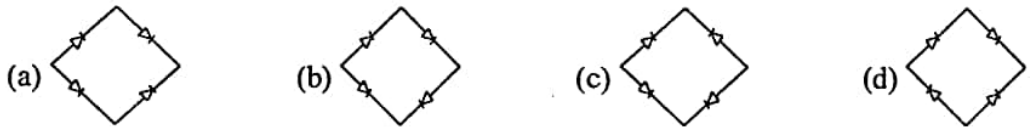
(d) low pass filter allowing $f < \frac{1}{2\pi\sqrt{LC}}$

75. Which of the following graphs correctly represents the frequency dependence of the gain G of a two-stage RC-coupled transistor amplifier?

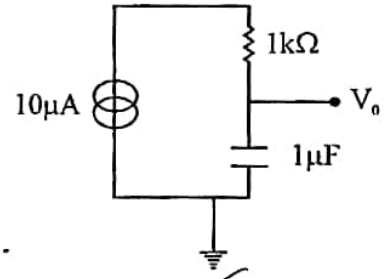


76. Given the full-wave rectifier circuit below, which is the correct configuration of the diodes?





77. In the following circuit the time required for V_0 to reach 1 Volt, starting from $V_0 = 0$ at $t = 0$, is



(a) 100 millisecond (b) 10 millisecond (c) 1 millisecond (d) 100 microsecond

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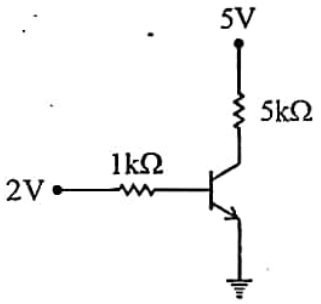
78. The Si transistor in the circuit shown below has $\beta = 100$.



The transistor is

(a) in saturation (b) in deep saturation (c) in cut off (d) in the linear region

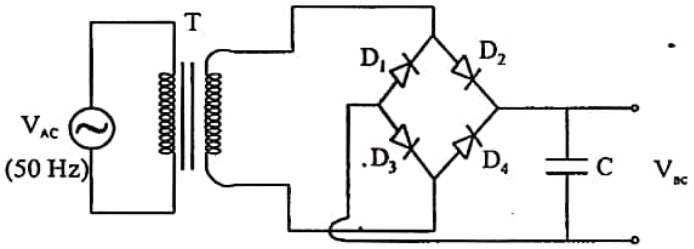
79. A comparator with hysteresis has

(a) no trigger points (b) one trigger point (c) two trigger points (d) a variable trigger point

80. The positive lead of an ohmmeter is connected to the anode of a diode and the negative lead is connected to the cathode. The diode then is

(a) short-circuited (b) reverse-biased (c) forward-baised (d) in avalanche breakdown

81. A DC power supply with a full wave bridge rectifier, a given in the figure below, shows a 50Hz ripple in the output voltage V_{DC}. The reason for the ripple is:



(a) the transformer secondary is shorted (b) the circuit is working properly.

(c) there is an open diode (d) the filter capacitor is leaky

82. A transistor can be used as a switching device when operated

(a) in the active region only (b) with both junctions either reverse or forward biased

(c) in the saturation region only (d) in the cut off region only

83. If the peak outoput voltage of a full wave rectifier is 10 V, its d.c. voltage is

(a) 10.0V (b) 7.07V (c) 6.36 V (d) 3.18V

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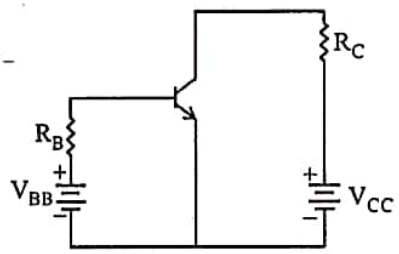
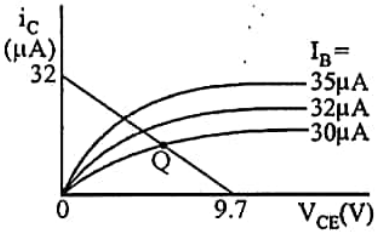
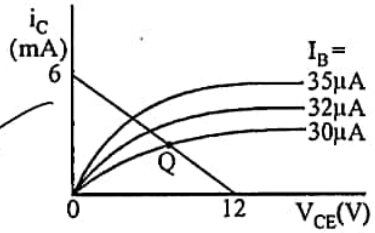
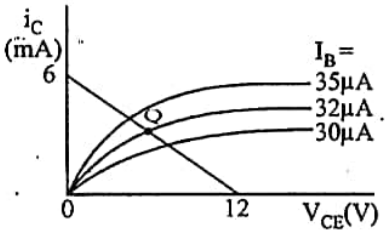
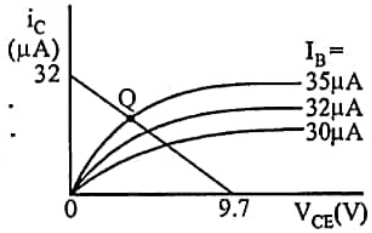
84. A silicon transistor with built-in voltage 0.7V is used in the circuit shown, with $V_{BB} = 9.7V$, $R_B = 300k\Omega$, $V_{CC} = 12V$ and $R_C = 2k\Omega$. Which of the following figures correctly represents the load line and the quiescent Q point?



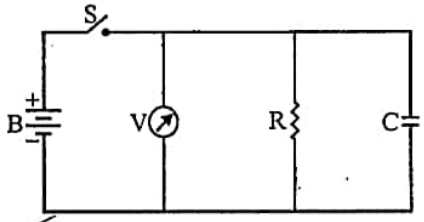
(a)


(b)


(c)


(d)


85. The insulation resistance R of an insulated cable is measured by connecting it in parallel with a capacitor C, a voltmeter, and battery B as shown. The voltage across the cable dropped from 150V to 15V, 1000 seconds after the switch S is closed. If the capacitance of the cable is 5μF then its insulation resistance is approximately



(a) $10^9\Omega$ (b) $10^8\Omega$ (c) $10^7\Omega$ (d) $10^6\Omega$

86. Which of the following statements are correct for basic transistor amplifier configurations?
(a) CB amplifier has low input impedance and a low current gain.
(b) CC amplifier has low output impedance and a low current gain.
(c) CE amplifier has very poor voltage gain but very high input impedance.
(d) The current gain of CB amplifier is higher than the current gain CC amplifier.

87. A triangular-square wave generator uses
(a) A sine wave oscillation and a comparator (b) An integrator and a comparator
(c) A differentiator and a comparator (d) A sine wave oscillator and a clipper.

88. An *n*-channel junction field effect transistor has 5*m*A source to drain current at shorted gate (I_{DSS}) and -5V pinch off voltage (V_p). Calculate the drain current in *m*A for a gate-source voltage (V_{GS}) of –2.5V. The answer should be up to two decimal places _____

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89. In a dual slope type digital voltmeter, an unknown signal voltage is integrated over 100 cycles of clock. If the signal has a 50 Hz pickup, the maximum clock frequency can be.
(a) 50 Hz (b) 5 KHz (c) 10 KHz (d) 50 KHz

Data for linked Q. 90 and Q. 91.
A dual slope ADC uses a 16-bit counter with a 5MHz, clock. if maximum input voltage is +12 volt and maximum integrator output voltage for maximum count is -10 volt. If resistor used in integrator is 100 KΩ. Then

90. What is conversion period of dual slope ADC
(a) 5ms (b) 10 ms (c) 13 ms (d) 26 ms

91. What is the value of capacitor used.
(a) 0.48 μF (b) 1 μF (c) 0.16 μF (d) 0.32 μF

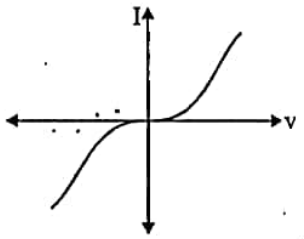
92. The conversion time of an 8-bit successive approximation counter with 1MHz clock is nearly
(a) 8 μsec. (b) 128 μsec. (c) 256 μsec. (d) 512 μsec.

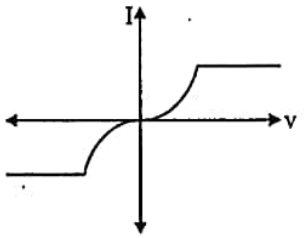
93. The largest analog output voltge from a 6-bit digital to analog converter (DAC) which produces 1.0 V output for a digital input of 010100, is:
(a) 1.6 V (b) 2.9 V (c) 3.15 V (d) 5.0 V

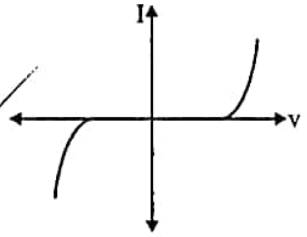
94. What should be the clock frequency of a 6-bit A/D converter so that its maximum conversion time is 32μs ?
(a) 1 MHz (b) 2 MHz (c) 0.5 MHz (d) 4 MHz

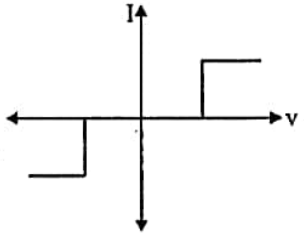
95. A voltage regulator has ripple rejection of –50dB. If input ripple is 1mV, what is the output ripple voltage in μV? The answer should be up to two decimal places _____

96. Two identical Zener diodes are placed back to back in series and are connected to a variable DC power supply. The best representation of the I-V characteristics of the circuit is

(a)


(b)


(c)


(d)


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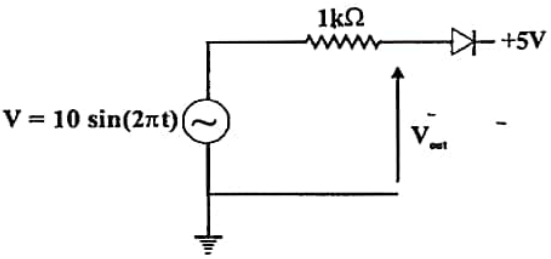
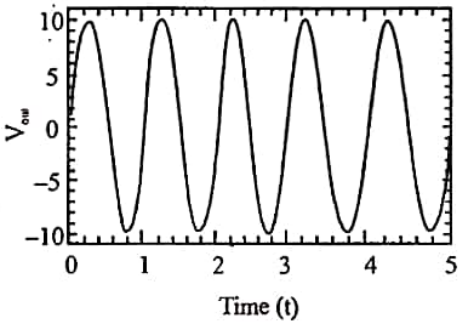
97. Consider the following circuit

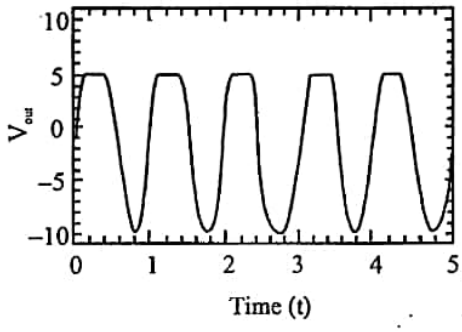


Which of the graphs given below is a correct representation of V_{out}?

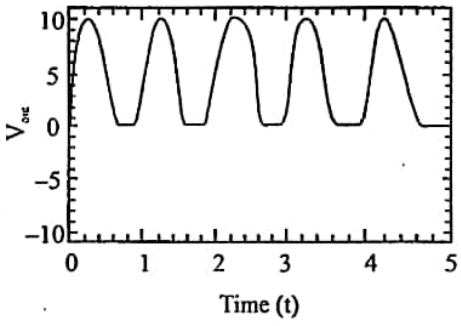
(a)



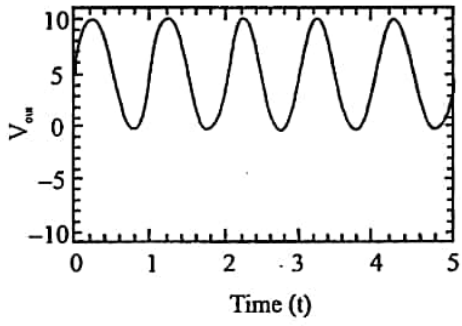
(b)



(c)



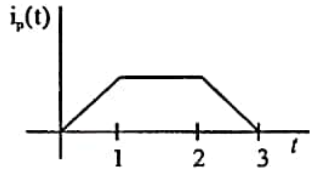
(d)



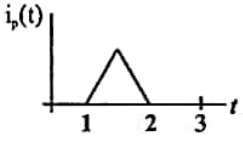
98. An RC network produces a phase-shift of 30°. How many such RC networks should be cascaded together and connected to a Common Emitter amplifier so that the final circuit behaves as an oscillator?

(a) 6 (b) 12 (c) 9 (d) 3

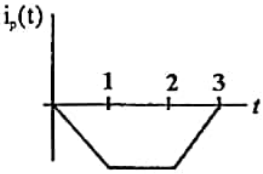
99. A current i_p flows through the primary coil of a transformer. The graph of $i_P(t)$ as a function of time 't' is shown in figure below



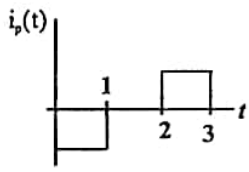
(a)



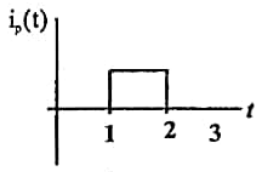
(b)



(c)



(d)



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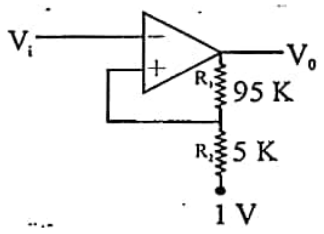
Assignment: OP-AMP

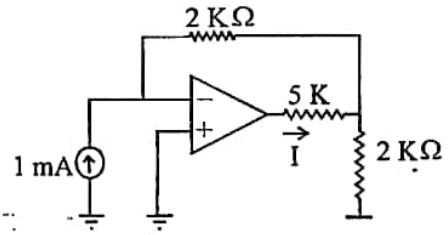
1. What is hysteresis voltage for a given Schmitt trigger circuit?

$V_{sat} = \pm 10\,V$



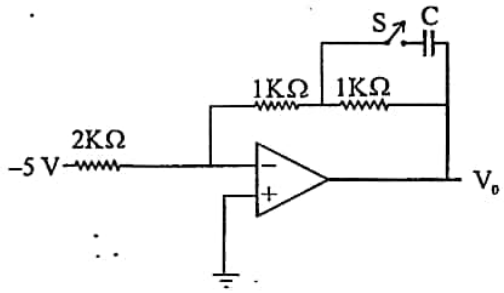
(a) 1 V (b) –1 V (c) 2 V (d) –2 V

2. Assume OP-AMP to be Ideal, what is value of current I, through 5KΩ resistor?



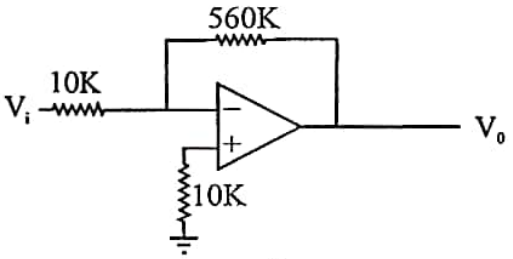
(a) 2mA (b) –2mA (c) 4 mA (d) –4 mA

3. What is value of output voltage when switch is closed? It is assumed that system is in steady state position?



(a) +5 (b) –5 (c) –2.5 (d) +2.5

4. The OP-AMP used in inverting amplifier show in figure has an equivalent input offset voltage of 5 mV. The total offset voltage is:



(a) 5 mV (b) –280 mV (c) –285 mV (d) 560 mV

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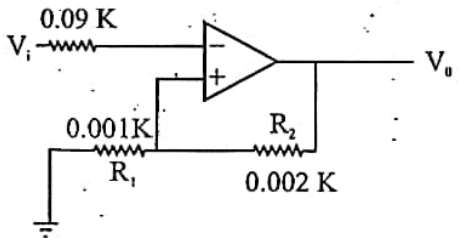
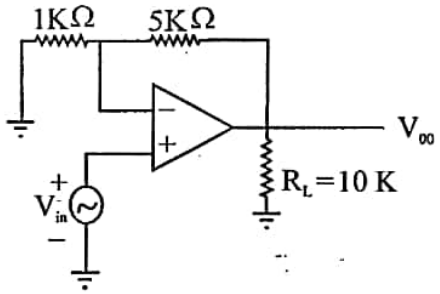
5. Feedback factor (β) of circuit is



$\beta = \frac{R_1}{R_1+R_2} = \frac{0.001}{0.003} = 0.33$

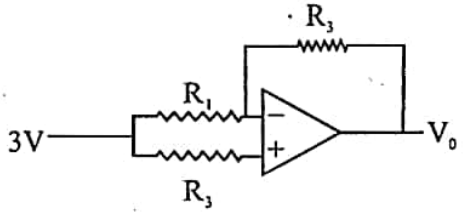
(a) 0.33 (b) 0.67 (c) Data is insufficient (d) 0.03

6. In case of circuit shown in figure, $V_{io} = 10$ mV D.C. The maximum possible output offset voltage V_{00}, caused by input voltage V_{io}, w.r.t. GND is:



(a) 60 volt D.C (b) 60 mV D.C (c) 110 volt D.C (d) 50 mV D.C

7. What is CMRR of given Op-Amp Circuit.



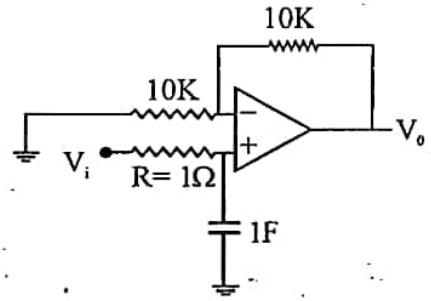
(a) 0 (b) 1 (c) ∞ (d) 3

8. For the above question, what is the value of output?

(a) 0 (b) 1

(c) 3 (d) Interms of R_1, R_2 & R_3

9. For given ideal OP-AMP if $V_i = \sin t$ What is the value of V_0?



(a) $\sqrt{2}\sin(t+45°)$ (b) $\sqrt{2}\sin(t-45°)$

(c) $1/\sqrt{2}\sin(t+45°)$ (d) $1/\sqrt{2}\sin(t-45°)$

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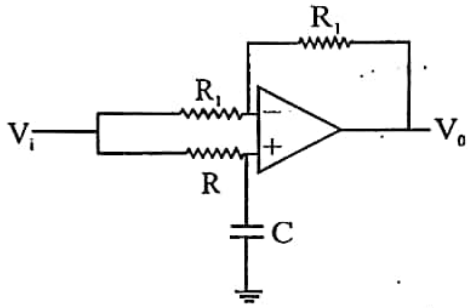
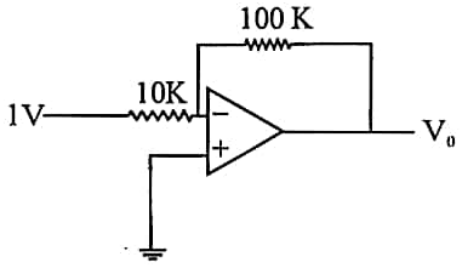
10. For the circuit shown in figure, with an ideal OP-AMP, what is the maximum phase shift of output with reference to input?



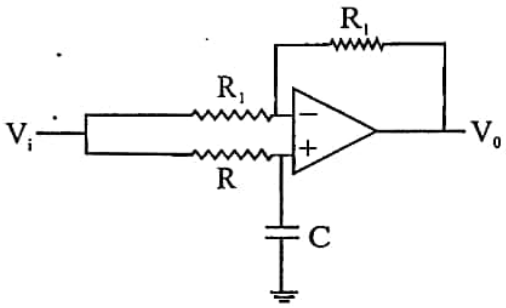
(a) 0° (b) 90° (c) –95° (d) $\pm 180°$

11. The inverting OP-AMP, shown in figure has an open loop gain of 50, What is value of closed loop gain?



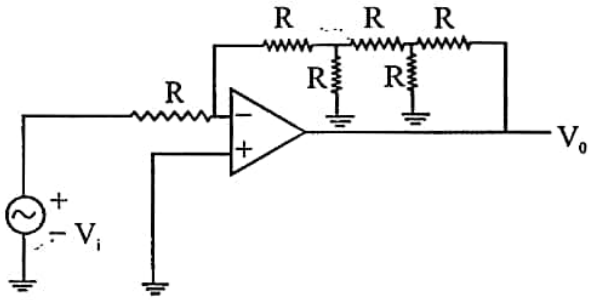
(a) –8 (b) –9 (c) –10 (d) +11

12. Calculate value of C if $\omega = 1000$ Rad /sec $R = 100K\Omega$, R_1 is 100Ω and phase shift between V_0 and V_i is 270°



(a) 1μF (b) 0.1 μF (c) 0.2 μF (d) 0.01 μF

13. What is the value of gain of given circuit?



(a) –4 (b) –7 (c) –9 (d) –8

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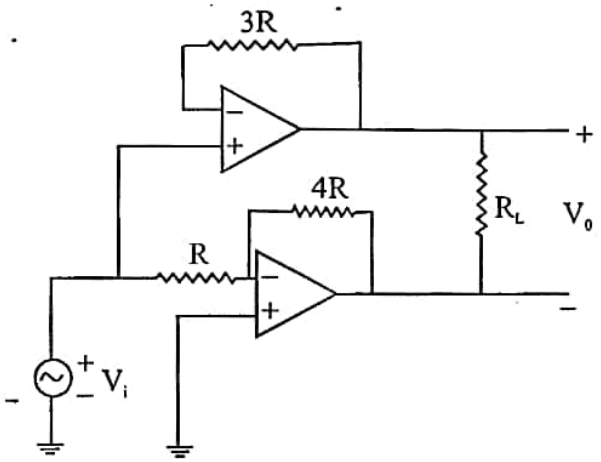
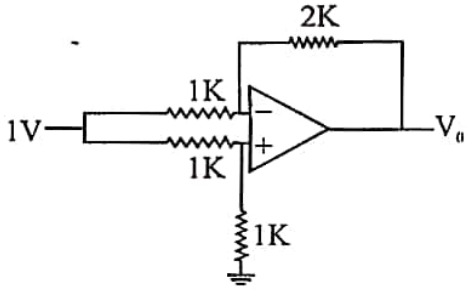
14. What is the value of gain V_0 / V_i of given circuit?



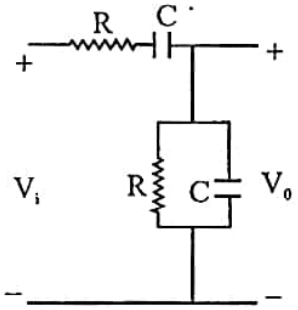
(a) +4 (b) 5 (c) 0 (d) $-3R_L / R$

15. For given OP-AMP what is value of output voltage V_0?



(a) –2V (b) –0.5V (c) –1V (d) 0.5 V

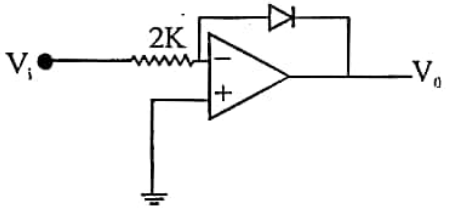
16. The RC, circuit shown in figure is?



(a) LPF (Low Pass Filter) (b) HPF (High Pass Filter)

(c) BPF (Band Pass Filter) (d) BSF (Band Stop Filter)

17. In the OP-AMP circuit shown, assume that diode current follows the equation $I = I_0 \exp(V / V_T)$. For $V_i = 2V$, $V_0 = V_{01}$ and for $V_i = 4V$, $V_0 = V_{02}$. Relationship between V_{01} & V_{02} is



(a) $V_{02} = \sqrt{2}\, V_{01}$ (b) $V_{02} = e^2 V_{01}$ (c) $V_{02} = V_{01} \ln 2$ (d) $V_{01} - V_{02} = V_T \ln 2$

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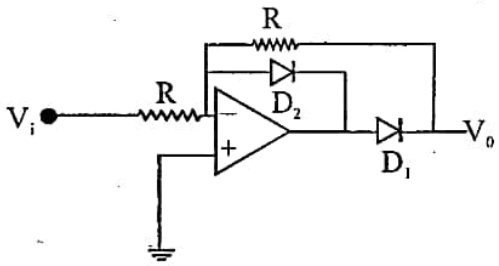
18. If OP-AMP is ideal and i/p is triangular wave then V_0 will be

(a) Sq. wave (b) Triangular (c) Parabolic (d) Sine

19. In circuit shown in figure, function of Diode D_2 is:



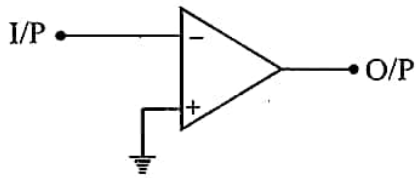
(a) to provide negative feedback when input in negative

(b) to avoid saturation of operational amplifier

(c) to reduce reverse berekdown voltage of diode D_1.

(d) In significant and can be removed.

20. If the input to the circuit of figure is sine wave the output will be



(a) A half-wave rectified sine wave (b) A full wave rectified sine wave

(c) A triangular wave (d) A square wave

21. The input to a lock-in amplifier has the form $V_i(t) = V_i \sin(\omega t + \theta_i)$ where V_i, ω, θ_i are the amplitude, frequency and phase of the input signal respectively. This signal is multiplied by a reference signal of the same frequency ω, amplitude V_r and phase θ_r. If the multiplied signal is fed to a low pass filter of cut-off frequency ω, then the final output signal is

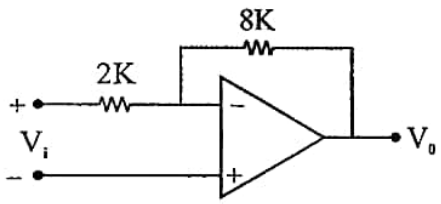
(1) $\frac{1}{2} V_i V_r \cos(\theta_i - \theta_r)$

(2) $V_i V_r \left[\cos(\theta_i - \theta_r) - \cos\left(\frac{1}{2}\omega t + \theta_i + \theta_r\right) \right]$

(3) $V_i V_r \sin(\theta_i - \theta_r)$

(4) $V_i V_r \left[\cos(\theta_i - \theta_r) + \cos\left(\frac{1}{2}\omega t + \theta_i + \theta_r\right) \right]$

22. The OP-AMP of figure has a very poor open loop voltage gain of 45 but is otherwise ideal. The gain of the amplifier equals.



(a) 5 (b) 20 (c) 4 (d) 4.5

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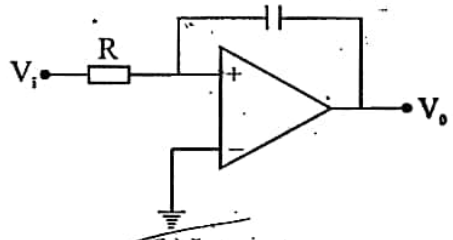
23. The circuit given below works as:



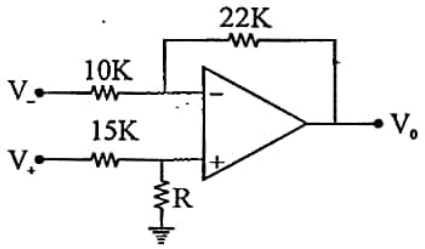
(a) Differentiator (b) Integrator
(c) Both as integrator and differentiator. (d) None of above.

24. Two non-inverting amplifiers, one having a unity gain and the other having a gain of twenty are made using identical operational amplifiers. As a compared to the unity gain amplifier, the amplifier with gain twenty has:
(a) Less negative feedback (b) Greater input impedance
(c) Less bandwidth (d) None of the above.

25. The input differential stage of OP-AMP 741 is biased at about 10 μA current. Such a low current of the input stage gives
1. High CMRR 2. High differential gain.
3. Low differential gain. 4. High input impedance
Which of these are correct?
(a) 1 and 2 (b) 1, 2 and 4 (c) 3 and 4 (d) 1, 2, 3 and 4

26. Negative feedback in amplifiers:
1. Improves the signal to noise ratio at the input.
2. Improves the signal to noise ratio at the output.
3. Does not affect the signal to noise ratio at the output.
4. Reduces distortion.
Then which of the following statements are correct:
(a) 1 and 2 only (b) 2 and 3 only (c) 2 and 4 only (d) 1, 2 and 4.

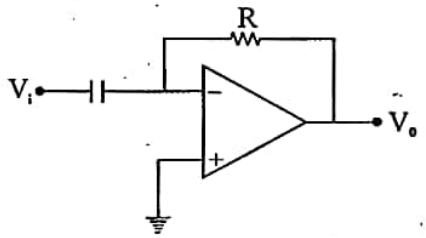
27. In the given circuit (figure) if the voltage inputs V_- and V_+ are to be amplified by the same amplification factor, the value of R should be:



(a) 66 K (b) 99 K (c) 33 K (d) 11 K

28. Negative feedback in voltage series configuration:
(a) Increase input impedance (b) Decease input impedance
(c) Increases closed loop gain (d) Leads to oscillation.

29. Assume that the OP-AMP of figure is ideal, if V_i is a triangular wave, then V_0 will be:



(a) Square wave (b) Triangular wave (c) Parabolic wave (d) Sine wave

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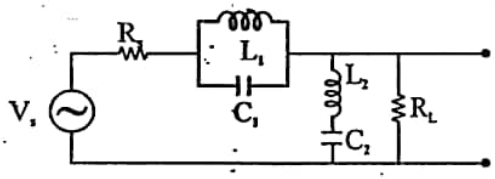
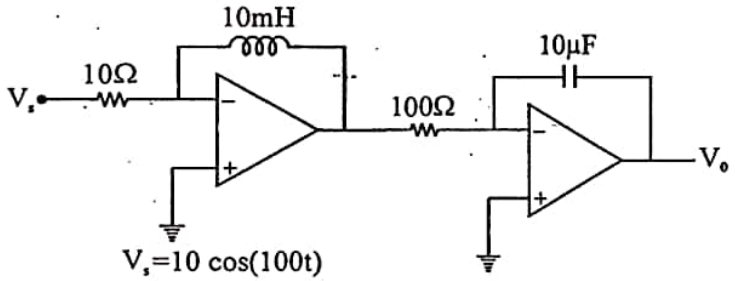
30. The circuit of figure represents a:



(a) Low pass filter (b) High pass filter (c) Band pass filter (d) Band reject filter.

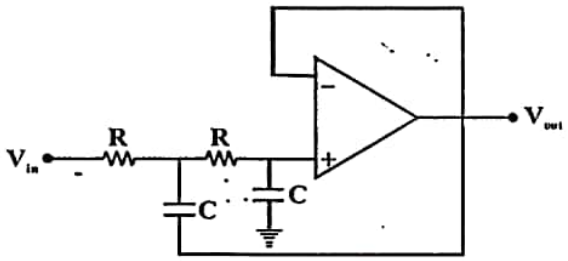
31. In figure assume the Op-Amps to be ideal. The output V_0 of the circuit is:



(a) 10 cos (100 t) (b) $10\int_0^t \cos(100\tau)\,d\tau$ (c) $10^{-4}\int_0^t \cos(100\tau)\,d\tau$ (d) $10^{-4}\frac{d}{dt}\cos(100t)$

32. An ideal OP-AMP is an ideal:
(a) Voltage controlled current source (b) Voltage controlled voltage source
(c) Current controlled current source (d) Current controlled voltage source.

33. The circuit in figure is a:



(a) Low-pass filter (b) High-pass filter (c) Band-pass filter (d) Band-reject filter

34. A differential amplifier has a differential gain of 20, 000. CMRR = 80 dB. The common mode gain is given by
(a) 2 (b) 1 (c) 0.5 (d) 0

35. Which of the following pairs is/are correctly matched?

Waveform	Circuitry and input signal
1. Triangular wave	Integrating circuit and square wave
2. Impulsive wave (Dirac Delta)	Differentiating circuit and step signal
3. Saw-tooth wave	Differentiating circuit and triangular wave

Select the correct answer using the codes given below:
(a) 2 and 3 (b) 1 and 2 (c) 1 alone (d) 1 and 3

36. An ideal OP-AMP has
(a) Infinite input and output impedance
(b) Very low input and output impedance
(c) Low input impedance and infinite output impedance
(d) Infinite input impedance and zero output impedance.

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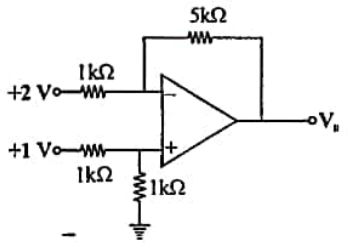
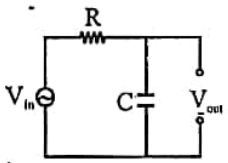
37. A differential amplifier is invariably used in the input stage of all OP-AMPs. This is done basically to provide the OP-AMPs with a very high
(a) CMRR (b) Bandwidth (c) Slew rate (d) Open-loop gain.

38. The output-V_0 of the ideal OP-AMP circuit shown in the figure is:



(a) –7V (b) –5 V (c) 5 V (d) 7 V

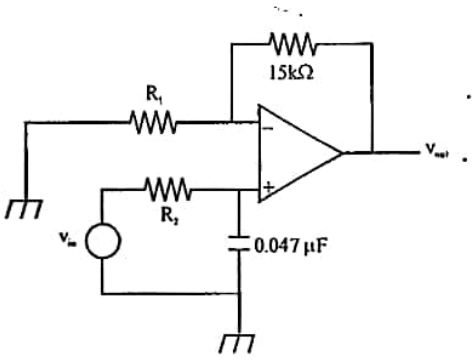
39. The circuit shown in the figure can be used as a



(a) High pass filter or a differentiator (b) High pass filter or an integrator
(c) Low pass filter or a differentiator (d) Low pass filter or an integrator.

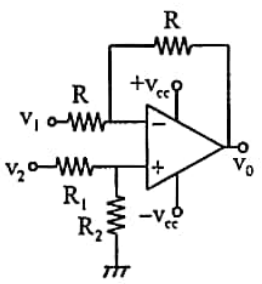
40. The low-pass active filter shown in the figure has a cut-off frequency of 2kHz and a pass band gain of 1.5. The values of the resistors are

(or) mid band
(or) pass band gain



(a) $R_1 = 10k\Omega; R_2 = 1.3\Omega$ (b) $R_1 = 30k\Omega; R_2 = 1.3\Omega$
(c) $R_1 = 10k\Omega; R_2 = 1.7\Omega$ (d) $R_1 = 30k\Omega; R_2 = 1.7\Omega$

41. In the following circuit, for the output voltage to $V_0 = (-V_1 + V_2/2)$ the ratio R_1/R_2 is



(a) 1/2 (b) 1 (c) 2 (d) 3

42. A power amplifier gives 150 W output for an input of 1.5W. The gain in dB, is:
(a) 10 (b) 20 (c) 54 (d) 100

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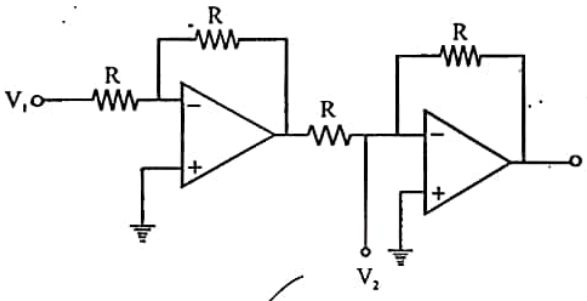
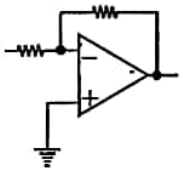
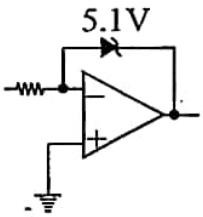
43. The circuit shown is based on ideal operational amplifiers. It acts as a

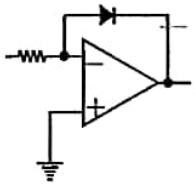


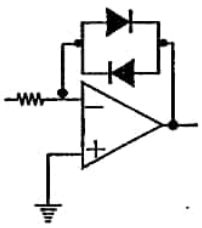
(a) Subtractor (b) Buffer amplifier (c) Adder (d) Divider.

44. In one of the following circuits, negative feedback does not operate for a negative input. Which one is it? The opamps are running from $\pm 15V$ supplies.

(a) 

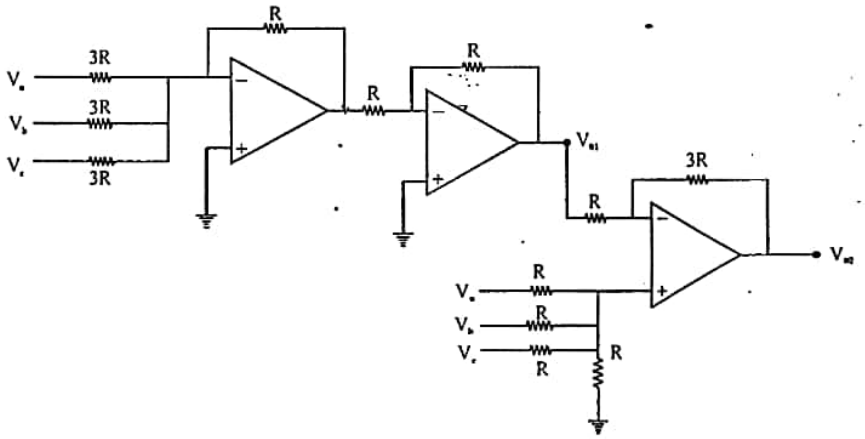
(b) 

(c) 

(d) 

Statement for Linked Answer Q.45 and Q.46

The following circuit contains three operational amplifiers and resistors.



45. The output voltage at the end of second operational amplifier V_{01} is:

(a) $V_{01} = 3(V_a + V_b + V_c)$ (b) $V_{01} = -\frac{1}{3}(V_a + V_b + V_c)$

(c) $V_{01} = \frac{1}{3}(V_a + V_b + V_c)$ (d) $V_{01} = \frac{4}{3}(V_a + V_b + V_c)$

46. The output V_{02} (at the end of third OP-AMP) of the above circuit is:

(a) $V_{02} = 2(V_a + V_b + V_c)$ (b) $V_{02} = 3(V_a + V_b + V_c)$

(c) $V_{02} = -\frac{1}{2}(V_a + V_b + V_c)$ (d) Zero.

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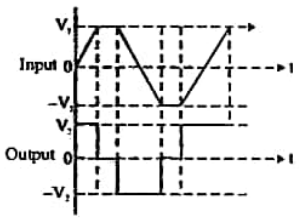
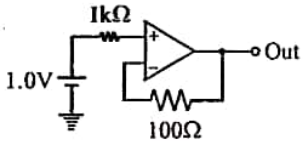
47. The circuit for which the input and output waveforms are shown below is:



(a) Clipping circuit (b) Integrator (c) Differentiation (d) Schmitt trigger.

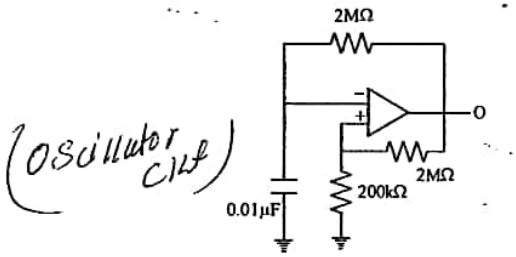
48. An operational amplifier
(a) Has a very high gain (b) Has a high input resistance
(c) Is a negative feedback amplifier (d) Has a very small input current.

49. The output of the circuit on the right will be



(a) 1V (b) 11V (c) –10V (d) 0 V

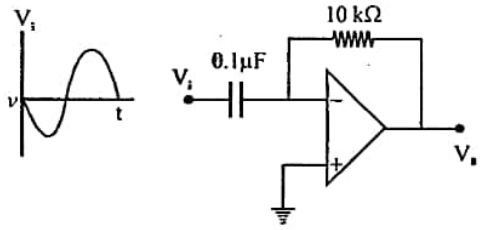
50. A multivibrator with a saturation voltage ±5V is shown in the diagram. The positive and negative threshold at the inverting terminal for which the multivibrator will switch to the other state are



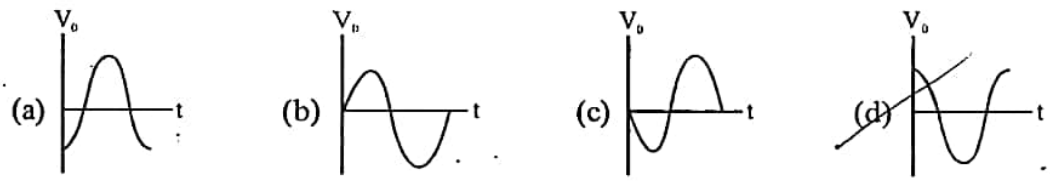
(a) ±5/11 V (b) ±10/11 V (c) ±5 V (d) ±11V

51. The inverting input terminal of an operational amplifier (OP-AMP) is shorted with the output terminal apart from being grounded. A voltage signal v_i is applied to the non-inverting input terminal of the op-amp. Under this configuration, the op-amp functions as
(a) An open loop inverter (b) A voltage to current converter.
(c) A voltage follower (d) An oscillator.

52. Consider the following operational amplifier circuit with an input signal of frequency 10 kHz.



Which of the following represents the output waveform V_0?



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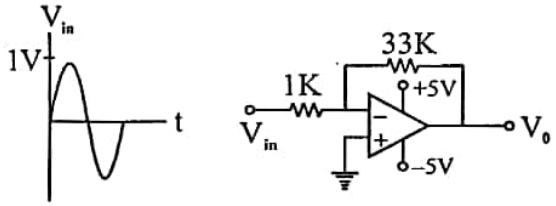
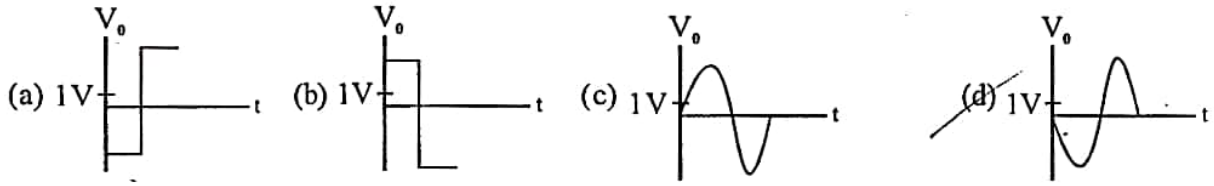
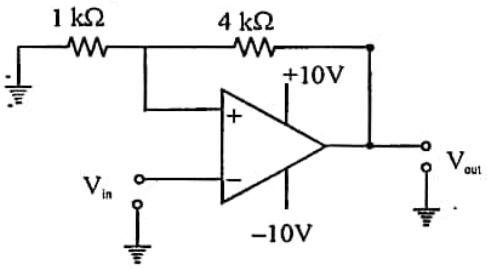
53. In an OP-AMP, when the input signal drives the output at a rate of voltage change greater than the slew rate, then the resulting signal.
(a) Is enchanced (b) Is clipped
(c) Is unaffected (d) Remains the same, but with 90° phase difference.

54. For the OP-AMP circuit shown in the figure below, which is the correct output waveform?

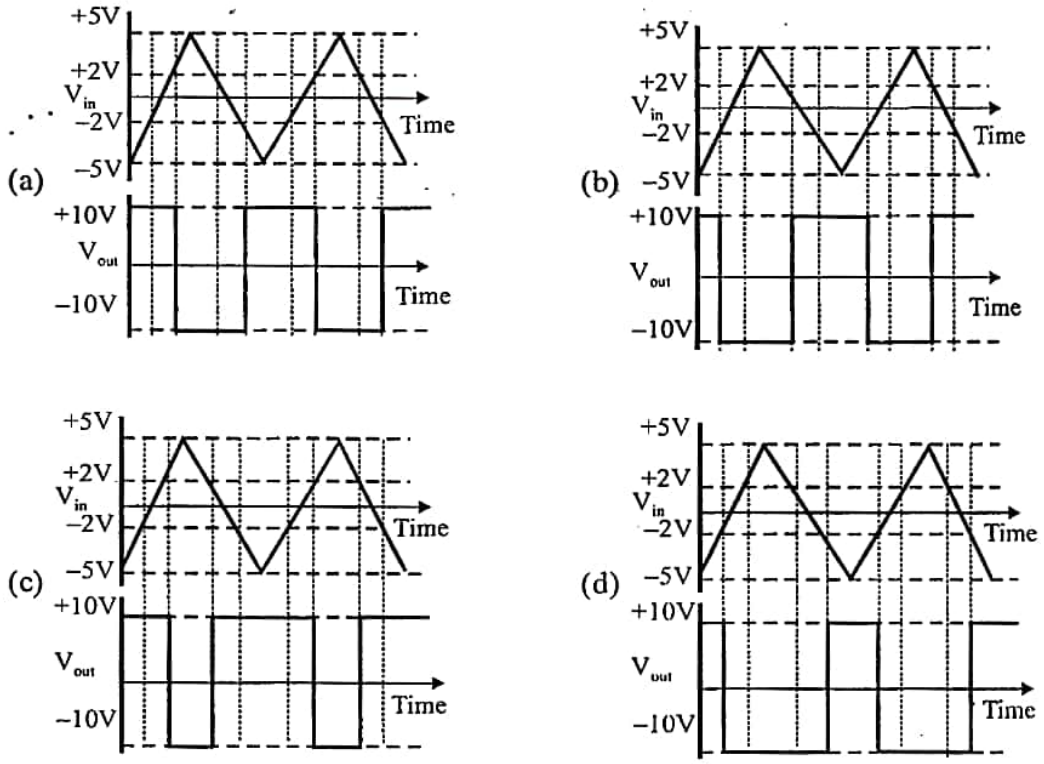




55. Consider the following circuit



Which of the following represents the output V_{out} corresponding to the input V_{in}?



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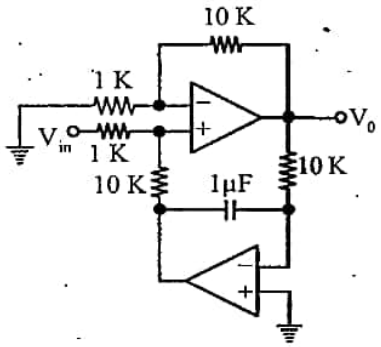
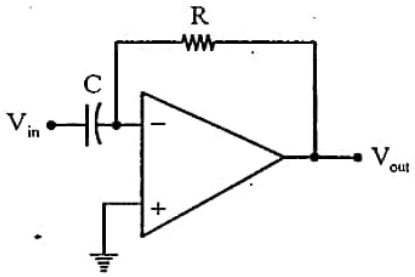
56. A time varying signal V_{in} is fed to an op-amp circuit with output signal V_0 as shown in the figure below. The circuit implements a

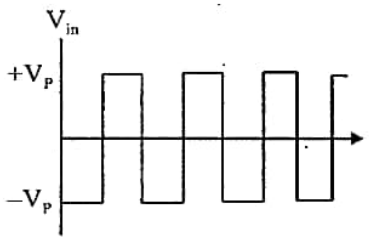


(a) High pass filter with cutoff frequency 16 Hz.
(b) High pass filter with cutoff frequency 100 Hz
(c) Low pass filter with cutoff frequency 16 Hz
(d) Low pass filter with cutoff frequency 100 Hz.

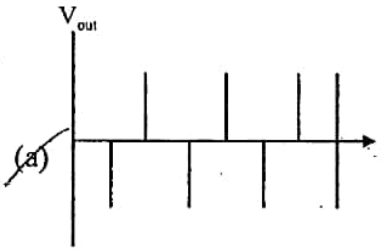
57. Consider the following circuit :

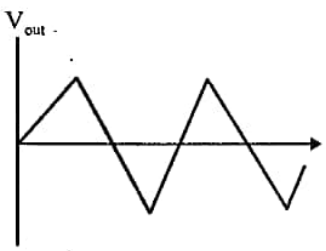


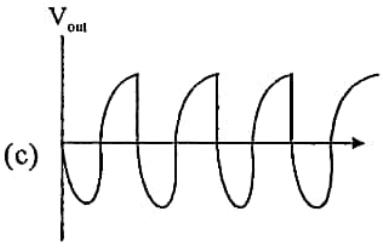
If the waveform given below is fed in at V_{in}

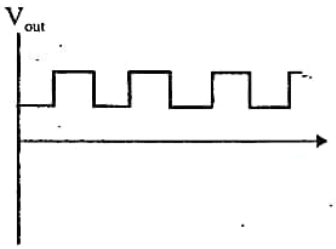


then the waveform at the output V_{out} will be

(a)


(b)


(c)


(d)


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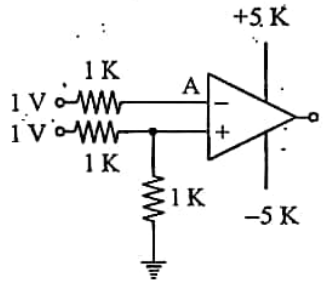
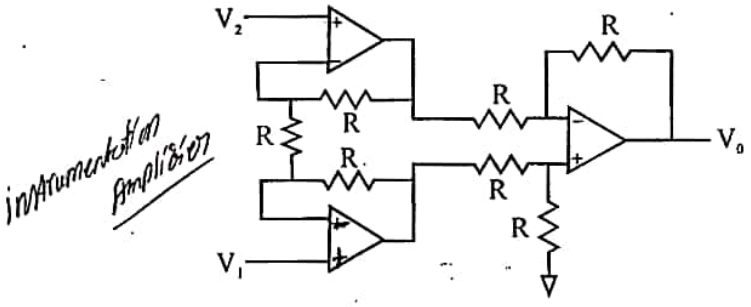
58. In the operational amplifier circuit below, the voltage at point A is



(a) 1.0 V (b) 0.5 V (c) 0 V (d) -5.0V

59. The classic there op-amp instrumentation amplifier configuration i shown below :



instrumentation amplifier

The ratio of maximum to minimum resistance that can be obtained with N $1-\Omega$ resistors is

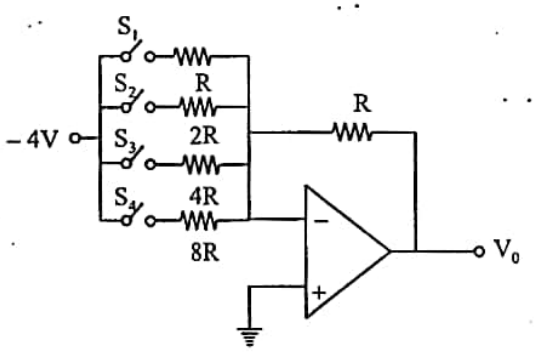
(a) N (b) N^2 (c) 1 (d) ∞

60. A triangular waveform is applied to the input of a differentiator. The output i

(a) a dc signal (b) a square waveform

(c) an inverted triangular waveform (d) the first harmonic of the triangular waveform

61. The circuit shown below implements a 4-bit DAC. Which of the switches S1,....., S4 should be closed to get an output voltge V_0 as close to 2.6V as possible?



(a) S1 and S4 (b) S2 nd S3 (c) S3 nd S4 (d) S2 and S4

62. A sinusoidal signal $V_i = V_P \sin(\omega t)$ is applied to the input of an op-amp with slew rate S_R. The op-amp maximum frequency ω_{max} that the op-amp can sustain without output distortion is:

(a) $\sqrt{2\pi}\, S_R / V_p$ (b) $S_R / 2V_p$ (c) $2S_R / V_p$ (d) S_R / V_p

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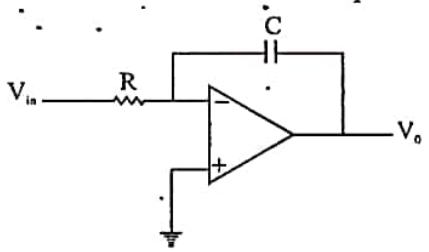
63. In the given operational amplifier circuit what is the correct expression for the output voltage?



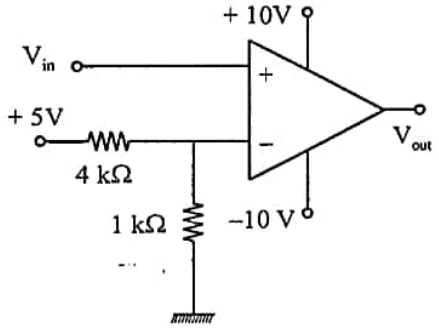
(a) $V_0 = -RC\frac{dV_{in}}{dt}$ (b) $V_0 = -\frac{1}{RC}\frac{dV_{in}}{dt}$ (c) $V_0 = -RC\int_{t=0}^{t} V_{in}dt$ (d) $V_0 = -\frac{1}{RC}\int_{t=0}^{t} V_{in}dt$

64. For a step input, the output of an integrator is a
(a) pulse (b) ramp (c) triangular wave from (d) spike

65. A certain inverting amplifier has a closed-loop gain of 25. The OP-AMP has an open-loop gain of 100000. If another OP-AMP with an open-loop gain of 300, 000 is substituted in the configuration, the closed-loop gain
(a) drops to 12.5 (b) doubles (c) remains at 25 (d) become $25\left(1-\frac{25}{200000}\right)$

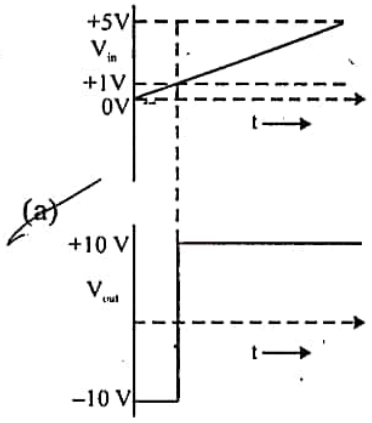
66. A signal of frequency 10 kHz is being digitized by an A/D converter. Which of the following is an appropriate value for the sampling time?
(a) 400 μs (b) 40 μs (c) 100 μs (d) 200 μs

67. Consider the following OP-AMP circuit.

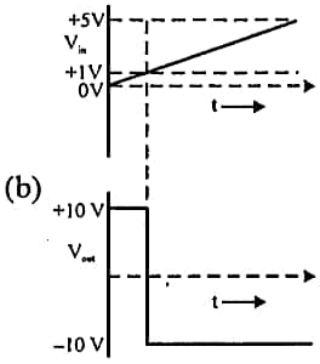


Which one of the following correctly represents the output V_{out} corresponding to the input V_{in} ?

(a)



(b)



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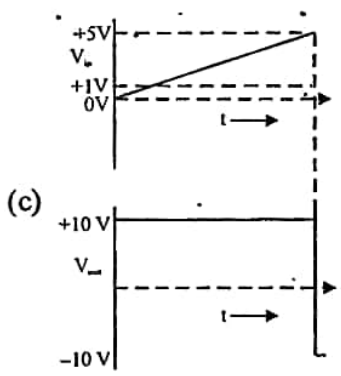
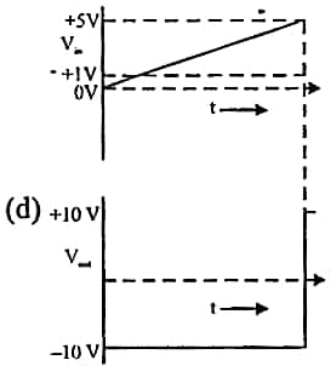
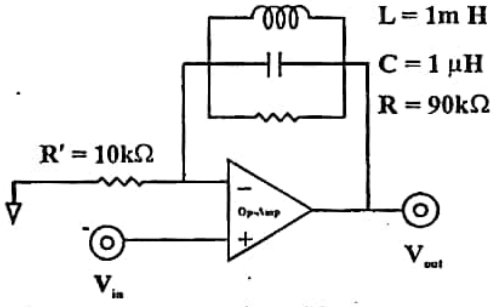


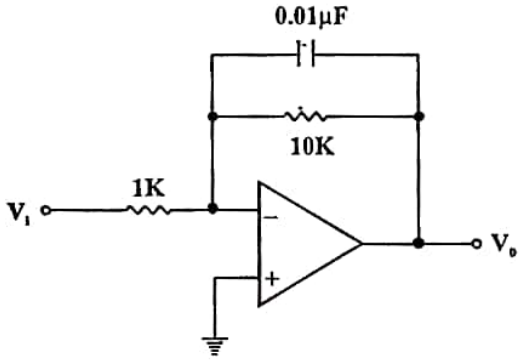


68. An input of 1.0 V DC is given to the ideal Op-Amp circuit depicted below. What will be the output voltage?



(a) 10.0 V (b) –9.0 V (c) 1.0 V (d) 0 V

69. In the op-amp circuit shown in the figure, V_i is a sinusoidal input signal of frequency 10 Hz and V_0 is the output signal.



The magnitude of the gain and the phase shift, respectively, are close to the values

(a) $5\sqrt{2}$ and $\frac{\pi}{2}$ (b) $5\sqrt{2}$ and $\frac{-\pi}{2}$ (c) 10 and zero (d) 10 and π

70. Band-pass and band-reject filters can be implemented by combining a low pass and a high pass filter in series and in parallel, respectively. If the cut-off frequencies of the low pass and high pass filters are ω_0^{LP} and ω_0^{HP}, respectively, the condition required to implement the band-pass and band-reject filters are respectively.

(a) $\omega_0^{HP} < \omega_0^{LP}$ and $\omega_0^{HP} < \omega_0^{LP}$ (b) $\omega_0^{HP} < \omega_0^{LP}$ and $\omega_0^{HP} > \omega_0^{LP}$

(c) $\omega_0^{HP} > \omega_0^{LP}$ and $\omega_0^{HP} < \omega_0^{LP}$ (d) $\omega_0^{HP} > \omega_0^{LP}$ and $\omega_0^{HP} > \omega_0^{LP}$

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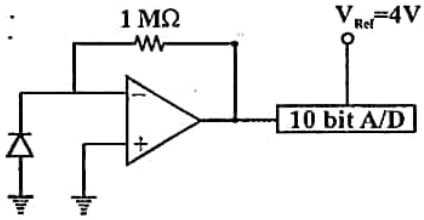
Statement for Linked Q.71 and Q.72.

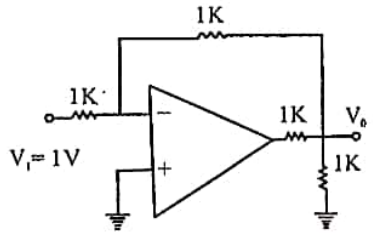
Shown in the figure is a circuit to measure light intensity and convert it to a digital signal. The photodiode P has a responsivity of 0.1A per watt of incident light intensity. The Op-amp converts the induced photocurrent to a voltage which is digitized by the 10-bit A/D converter with a reference voltage of 4V.



71. For a light intensity of 25 μW incident on the photodiode, the voltage output of the OP-amp is:
(a) 0.25 V (b) 1.0 V (c) 4.0 V (d) 2.5 V

72. The range of light intensity which can be measured by this set up is:
(a) 100 nW to 100μW (b) 100 nW to 100μW
(c) 40 nW to 40μW (d) 40 nW to 40μW

73. In the op-amp circuit shown in the figure below, the input voltage V_i is 1V. The value of the output V_0 is:

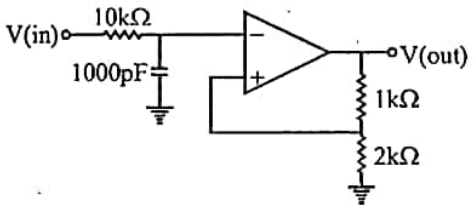


(a) –0.33 V (b) –0.50 V
(c) –1.00 V (d) –0.25 V

74. If the analog input to an 8-bit successive approximation ADC is increased from 1.0 V to 2.0 V, then the conversion time will
(a) remain unchanged (b) double
(c) decrease to half its original value (d) increase four times

Statement for Linked Answer Q. 75 and Q. 76 :

Consider the following circuit



75. For this circuit the frequency above which the gain will decrease by 20dB per decade is
(a) 15.9 kHz (b) 1.2 kHz (c) 5.6 kHz (d) 22.5 kHz

76. At 1.2 kHz the closed loop gain is
(a) 1 (b) 1.5 (c) 3 (d) 0.5

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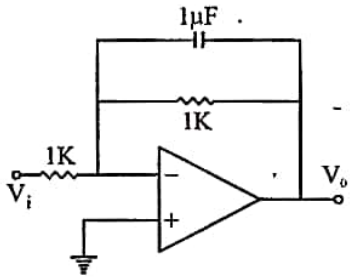
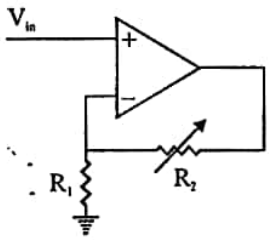
77. Consider the op-amp circuit shown in the figure.



If the input is a sinusoidal wave $V_i = 5\sin(1000t)$, then the amplitude of the output V_0 is

(a) $\frac{5}{2}$ (b) 5 (c) $\frac{5\sqrt{2}}{2}$ (d) $5\sqrt{2}$

78. In the following circuit, the resistance R_2 is doubled.



It follows that the current through R_2.

(a) remains the same (b) is halved

(c) is doubled (d) is quadrupled.

79. An op-amp based voltage follower

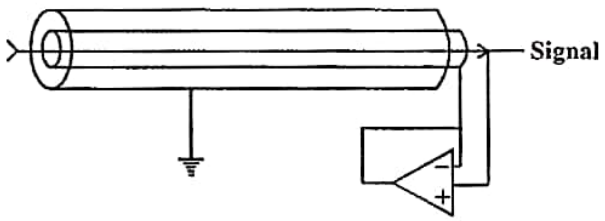
(a) is useful for converting a low impedance source into a high impedance source

(b) is useful for converting a high impedance source into a low impedance source

(c) has infinitely high closed loop output impedance

(d) has infinitely high closed loop gain

80. The inner shield of a triaxial conductor is driven by an (ideal) op-amp follower circuit as shown. The effective capacitance between the signal-carrying conductor and ground is



(a) unaffected (b) doubled (c) halved (d) made zero

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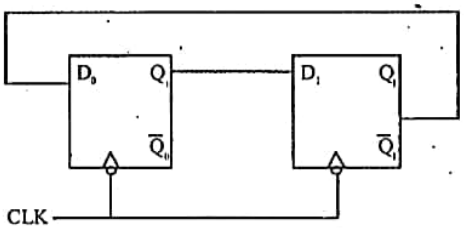
Assignment – Digital Electronics

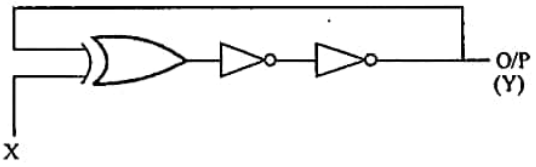
1. In the circuit shown below initially



$Q_0 = Q_1 = 0$, then what are the values of Q_0 and Q_1 after 335th clock pulse.

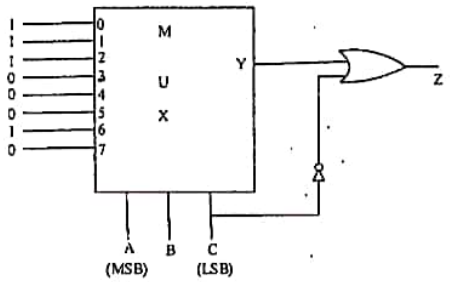
(a) 11 (b) 10 (c) 01 (d) 00

2. All the logic gates in circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



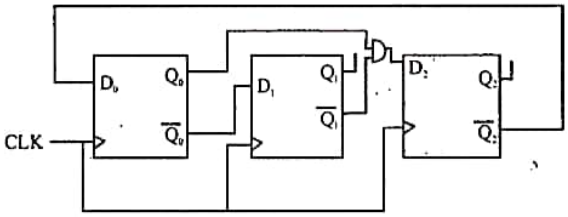
(a) X = 0 (b) X = 1 (c) X = 0 or 1 (d) $X = \overline{Y}$

3. A combinational circuit, using 8×1 MUX is shown in figure. The minimised expression for output Z is



(a) $C(\overline{A} + \overline{B})$ (b) $C(A + B)$ (c) $\overline{C} + \overline{AB}$ (d) $\overline{C} + \overline{A}\,\overline{B}$

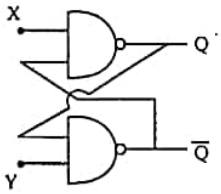
Data for linked Q.4 and Q.5:



4. Determine MOD of given counter

(a) 4 (b) 5 (c) 6 (d) 7

5. For a Flip-flop formed from 2 NAND gates as shown in figure, the unusable state corresponds to



(a) X = 0, Y = 0 (b) X = 1, Y = 0 (c) X = 0, Y = 1 (d) X = 1, Y = 1

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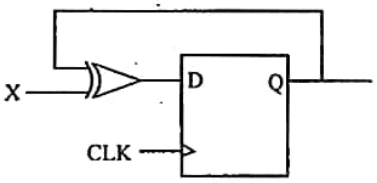
6. The minimal product of sums function described by K-Map, shown in figure is

C \ AB	00	01	11	10
C 1	1	1	×	0
C' 0	0	0	×	0

(a) A'C' (b) A'+C' (c) A+C (d) A'C

7. The Digital circuit shown in figure acts as a



(a) JK Flip flop (b) Clocked RS Flipflop (c) T Flipflop (d) Ring Counter

8. The open collector outputs of 2 inputs NAND gate are connected to a common pull up resistor if the inputs to gate are P, Q and R, S respectively. Then what is the value of output.

(a) $\overline{PQ}.\overline{RS}$ (b) $\overline{PQ}+\overline{RS}$ (c) PQ + RS (d) PQ.RS

9. The minimum no. of 2 inputs NAND gate required to implement boolean function f(A, B, C, D) = $A\bar{B}CD$ are

(a) 3 (b) 5 (c) 6 (d) 8

Date for linked Q.10 and Q.11.

The 4, variable function f is given in terms of min term as $f(A,B,C,D) = \sum(2,3,8,10,11,12,14,15)$. If by use of K-Map, function is minimised in sum of product forms, then SOP is

10. (a) $A\bar{D}+AC+\bar{B}C$ (b) $AD+\bar{A}C+BC$ (c) $\bar{A}D+AC+B\bar{C}$ (d) $AC+\bar{B}C$

11. Above minimised SOP, can be implemented by how many minimum no. of 2 inputs NAND gate:

(a) 6 (b) 7 (c) 8 (d) 9

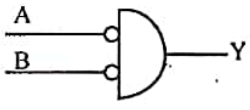
12. If 2's complement representation of a 16-bit number (one-sign bit and 15 magnitude bits) is FFFF, then its magnitude in decimal representation is

(a) 0 (b) 1 (c) 32767 (d) 65535

13. The initial state of MOD-16, down counter is 0110. What state will be it be after 37 clock pulses?

(a) Indeterminate (b) 0110 (c) 0101 (d) 0001

14. The negative logic AND gate shown in figure is equivalent to a positive logic



(a) AND gate (b) OR gate (c) NOR gate (d) NAND gate

15. How many min-terms (excluding redundant) does the minimal switching function

f(A, B, C, D, E) = C + $\overline{DE}$, originally have

(a) 16 (b) 20 (c) 24 (d) 32

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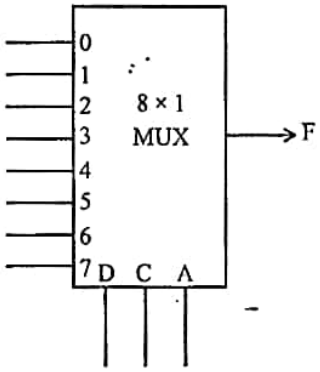
Data for linked Q.16 and Q.17.

The logic function f(A, B, C, D) = AC + ABD + ACD is to be realised using an 8 ×1 MUX

16. Shown in figure to realise this logic I_3, I_4, I_5 must be connected to



(a) 1, 0 , 0 (b) 1, 0, B (c) 0, 1, B (d) B, B, B

17. Can the function be realise using a 4×1, MUX

(a) Yes always

(b) No

(c) Yes, using some combinational ckt. we can realise

(d) Data not sufficient

18. The binary no. 110011 is to be converted to gray code, then no. of gates and type required are

(a) 6, AND (b) 6, XNOR (c) 6, XOR (d) 5, XOR

19. What is F'S complement of $(2BFD)_{16}$

(a) E304 (b) D402 (c) D403 (d) C403

20. If x and y are boolean variables then which one of the following is equivalent to $x \oplus y \oplus xy$

(a) $x + y$ (b) $x + \bar{y}$ (c) $\bar{x} + \bar{y}$ (d) $\bar{x} + y$

21. Any combinational circuit can be built using

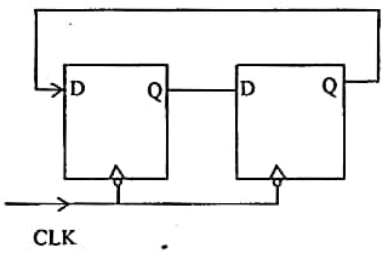
1. NAND 2. NOR 3. EX-OR 4. MUX

(a) 1, 2. (b) 1,2,3 (c) 1, 2, 4 (d) 1, 2, 3 4

22. A, MOD-11, ripple counter consists of 4 flipflops and a combinational circuit then economical combinational CKT. will be

(a) 4 input AND gate (b) 4 input NAND gate (c) 3 input OR gate (d) 3 input NOR gate

23. Above circuit represent a



(a) MOD-2 counter (b) MOD-3 counter (c) MOD-4 counter (d) MOD-4, ring counter.

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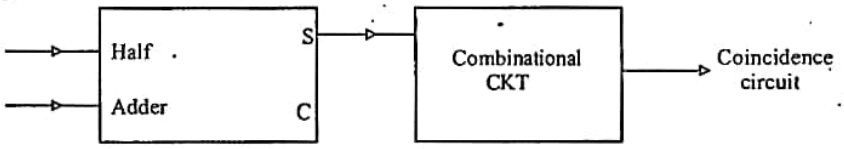
24. For given combinational circuit if output is coincidence circuit, then unknown combinational circuit is



(a) AND gate (b) OR gate (c) EXNOR gate (d) NOR gate

25. A, shift register can be made by use of

1. DFF 2. RSFF 3. TFF 4. JKFF

(a) 1,2,3 (b) 1, 3, 4 (c) 1, 4 (d) 1,2,4

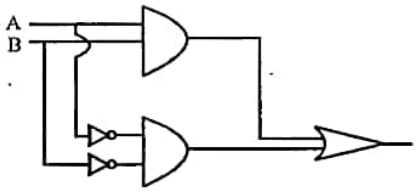
26. If an 8-bit 2's complement representation of an integer is FA (hex), then its decimal equivalent is

(a) –6 (b) +6 (c) –10 (d) +10

27. $(7E)_H$ and $(5F)_H$ are XOR. If output is multiplied by $(10)_H$ then result is:

(a) $(0210)_H$ (b) $(7EF5)_H$ (c) $(7FE5)_H$ (d) $(2100)_H$

28. The logic circuit shown in figure is:



(a) Half adder (b) X-OR gate (c) Equality detector (d) Full adder.

29. In a dual slope ADC, if reference voltage is 100 mV and the first integration period is set as 50 msec. For an input voltage of 120 mV, what is the second integration (de-integration) period.

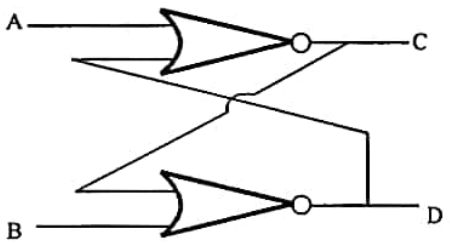
(a) 50 ms (b) 60 ms (c) 100 ms (d) 120 msec

30. If 2 4-bit 2's complement no's 1011 and 0110 are added, then result expressed in 2's complement notation is

(a) 0001 (b) 0010

(c) 1101 (d) cannot be expressed in 4 bit 2's complement

31. In circuit, shown in figure, when inputs A = B = 0, then possible logic states of C & D are



(a) C = 0, D = 1 or C = 1, D = 0 (b) C = 1, D = 1 or C = 0, D = 0

(c) C = 1, D = 0 (d) C = 0, D = 1

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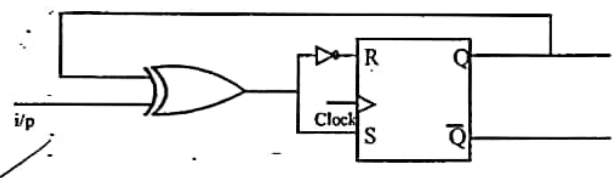
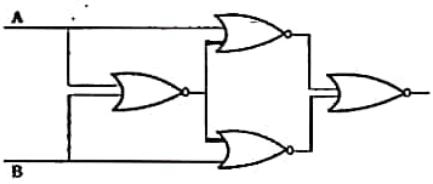
32. Given Digital circuit behaves as a



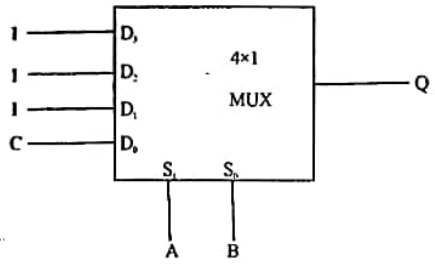
(a) D FF (b) T FF (c) JK FF (d) RS FF

33. Above given combinational circuit is equivalent to :



(a) NOR (b) OR (c) EX-OR (d) EX-NOR

34. The combinational circuit shown employs a 4×1, MUX, what is output Q of CKT.



(a) $\overline{A}+\overline{B}+C$ (b) $A+B+C$ (c) $A \oplus B \oplus C$ (d) $\overline{ABC}$

35. The boolean expression $f(P, Q, R) = \pi(0, 5)$ is to be realised using only two 2,input gates, what are these gates.

(a) AND & OR (b) NAND & OR (c) AND & XOR (d) OR & XOR

36. The boolean function $(x+y)(\overline{x}+z)(y+z)$ is equal to which one of the following expression

(a) $(x+y)(y+z)$ (b) $(\overline{x}+z)(y+z)$ (c) $(x+y)(\overline{x}+z)$ (d) $(x+y)(x+\overline{z})$

37. If output of a 2-level AND-OR network is F. What is the output when all gates are replaced by NOR gates.

(a) F (b) $\overline{F}$ (c) F_D (d) $\overline{F}_D$

38. The total no. of 1's in a 15-bit shift register is to be counted by clocking into a counter, which is present to O. The counter must have which one of the following.

(a) 4-bit (b) 5-bit (c) 6-bit (d) 16-bit

39. A number is expressed in binary 2's complement as 10011. Its decimal equivalent value is

(a) –19 (b) +19 (c) –13 (d) +13

40. The output voltage of a 5-bit DAC, binary ladder, which has a digital input of 11010 (assume O = 0V and 1 = +10 V) is:

(a) 3.4375 volt (b) 6.0 volt (c) 8.125 volt (d) 9.6875 volt

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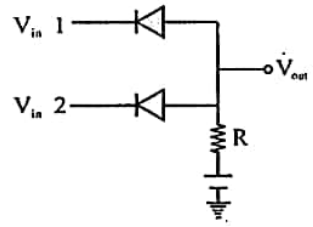
41. The circuit shown can be used as

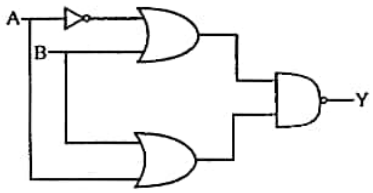


(a) NOR gate (b) OR gate (c) NAND gate (d) AND gate

42. The Boolean expression: $B(A+B)+A.(\overline{B}+A)$ can be realized using minimum number of

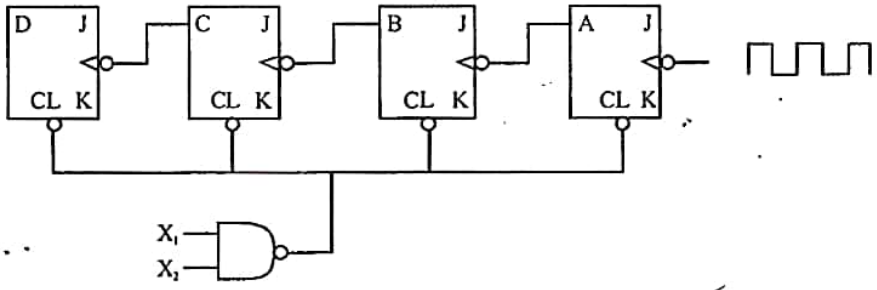
(a) 1 AND gate (b) 2 AND gates (c) 1 OR gate (d) 2 OR gates.

43. In the given digital logic circuit, A and B form the input. The output Y is:



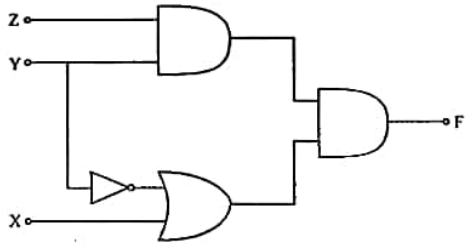
(a) $Y=\overline{A}$ (b) $Y=A\overline{B}$ (c) $Y=A+B$ (d) $Y=\overline{B}$

44. A ripple counter designed with JK flip-flops provided with CLEAR (CL) input is shown in the figure. In order that this circuit functions as a MOD-12 counter, the NAND gate input (X_1 and X_2) should be



(a) A and C (b) A and D (c) B and D (d) C and D

45. Identify the function F generated by the logic network shown



(a) $F=(X+Y)Z$ (b) $F=Z+Y+\overline{Y}X$ (c) $F=ZY(Y+X)$ (d) $F=XYX$

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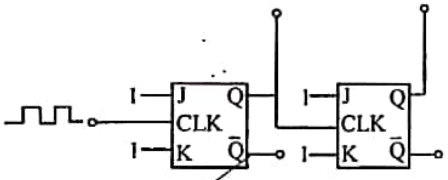
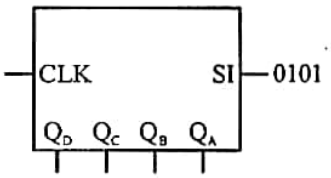
46. In the circuit shown, the ports Q_1 and Q_2 are in the state $Q_1 = 1$, $Q_2 = 0$. The circuit is now subjected to two complete clock pulses. The state of these ports now becomes



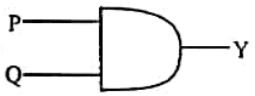
(a) $Q_2 = 1, Q_1 = 0$ (b) $Q_2 = 0, Q_1 = 1$ (c) $Q_2 = 1, Q_1 = 1$ (d) $Q_2 = 0, Q_1 = 0$

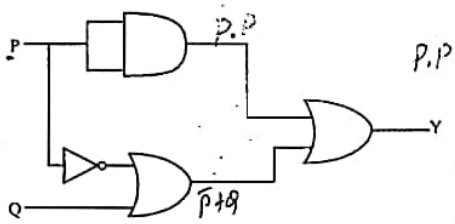
47. The registers Q_D, Q_C, Q_B and Q_A shown in the figure are initially in the state 1010 respectively. An input sequence SI=0101 is applied. After two clock pulses, the state of the shift registers (in the same sequence $Q_D\ Q_C\ Q_B\ Q_A$) is:

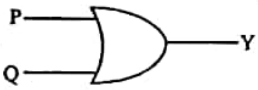


(a) 1001 (b) 0100 (c) 0110 (d) 1010

48. The simplest logic gate circuit corresponding to the Boolean expression, $Y = P + PQ$ is :

(a)


(b)


(c)


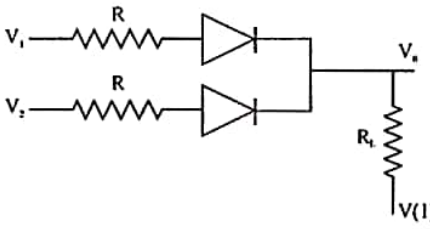
(d) None of these

49. An analog voltage V is converted into 2-bit binary number. The minimum number of comparators required and their reference voltages are

(a) $3, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{4}\right)$ (b) $3, \left(\frac{V}{3}, \frac{2V}{3}, V\right)$

(c) $4, \left(\frac{V}{5}, \frac{2V}{5}, \frac{3V}{5}, \frac{4V}{5}\right)$ (d) $4, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{5}, V\right)$

50. The following circuit (where $R_L >> R$) performs the operation of



(a) OR gate for a negative logic system (b) NAND gate for a negative logic system.
(c) AND gate for a positive logic system. (d) AND gate for a negative logic system.

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Statement for Linked Q.51 and Q.52.

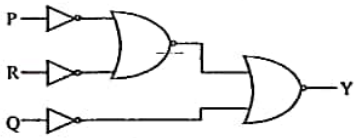
The karnaugh map of a logic circuit is shown below:

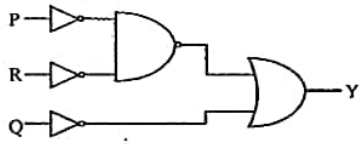
	$\bar{R}$	R
$\bar{P}\bar{Q}$	1	1
$\bar{P}Q$	1	
PQ		
$P\bar{Q}$	1	1

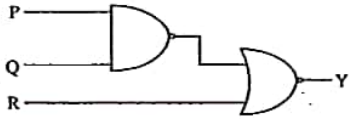
51. The minimized logic expression for the above map is:

(a) $Y = \bar{P}\bar{R} + \bar{Q}$ (b) $Y = \bar{Q}.PR$ (c) $Y = \bar{Q} + PR$ (d) $Y = Q.\overline{PR}$

52. The corresponding logic implementation using gates is given as:

(a) 

(b) 

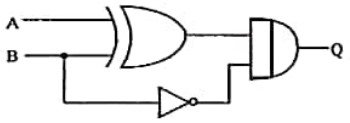
(c) 

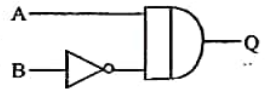
(d) None of the above

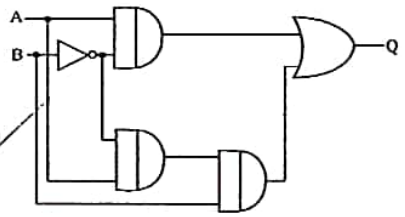
53. The voltage resolution of a 12-bit digital to analog converter (DAC), whose output varies from –10 V to + 10V is, approximately

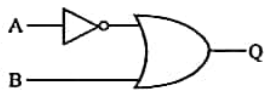
(a) 1 mV (b) 5 mV (c) 20 mV (d) 100 mV

54. For any set of inputs, A and B, the following circuits give the same output Q, except one. Which one is it?

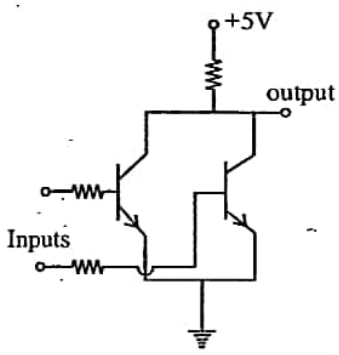
(a) 

(b) 

(c) 

(d) 

55. The circuit shown in figure below acts as a



(a) NOR gate (b) NAND gate
(c) AND gate (d) XOR gate

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56. In a logic circuit the output Y in terms of inputs A, B, C is $Y = ABC + A\bar{B}C + AB\bar{C}$. This circuit can be replaced by another logic circuit having.

(a) $Y = ABC$ (b) $Y = A(B+C)$ (c) $Y = B(A+C)$ (d) $Y = C(A+B)$

57. 10101 binary number corresponds to decimal number

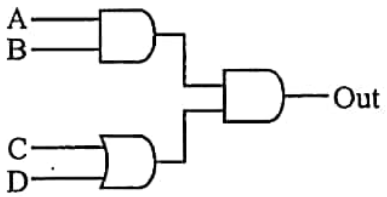
(a) 31 (b) 21 (c) 11 (d) 3

58. The basic memory element in a digital circuit

(a) Consists of a NAND gate (b) Consists of a NOR gate

(c) Is a FLIP-FLOP (d) Is a shift register.

59. If the output of the logic circuit shown in the figure is 1, the input could be



(a) A = 1, B = 1, C = 1, D = 0

(b) A =1, B = 1, C = 0, D = 0

(c) A = 1, B = 0, C = 1, D = 1

(d) A = 0, B = 1, C = 1, D = 1.

60. Which of the following options is true for a two input XOR gate?

	Input		Output
	A	B	
(a)	0	1	1
(b)	1	0	0
(c)	0	0	1
(d)	1	1	1

61. Which of the given relations between the Boolean variables P and Q is NOT correct? (In the notation used here, P′ denotes NOT P and Q′ denotes NOT Q)

(a) $PQ' + PQ = P$ (b) $(PQ)' = P' + Q'$ (c) $PQ' = (P' + Q)'$ (d) $PQ' + Q = P$

62. A half-adder is a digital circuit with

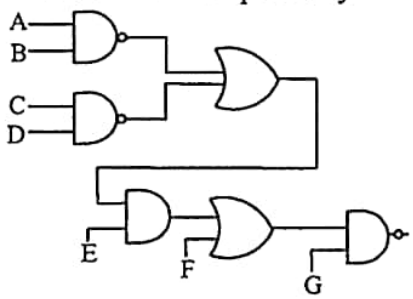
(a) Three inputs and one output (b) Three inputs and two outputs

(c) Two inputs and one output (d) Two input and two outputs.

63. The output 0, of the given circuit in cases I and II, where

Case-I: A, B = 1; C, D = 0; E, F = 1 and G = 0

Case-II: A,B = 0; C, D = 0; E, F = 0 and G = 1 are respectively



(a) 1, 0 (b) 0, 1 (c) 0, 0 (d) 1, 1

64. Which of the following logic families has the highest speed.

(a) DTL (b) TTL (c) CMOS (d) ECL

65. Five panelists are required to elect a sixth member to the panel. If any of the panelists votes againt a member, the member is disqualified. What would be the appropriate electronic circuit to be used in the electronic voting machine to implement the above rule?

(a) XOR (b) XNOR (c) OR (d) AND

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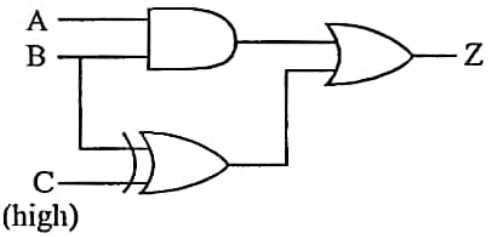
66. The following Boolean expression

$Y = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot B \cdot C \cdot D + A \cdot \bar{B} \cdot \bar{C} \cdot D$ can be simplified to

(a) $\bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{D}$ (b) $\bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{D}$ (c) $A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot D$ (d) $A \cdot \bar{B} \cdot C + \bar{A} \cdot D$

67. Consider the digital circuit shown below in which the input C is always high (I).



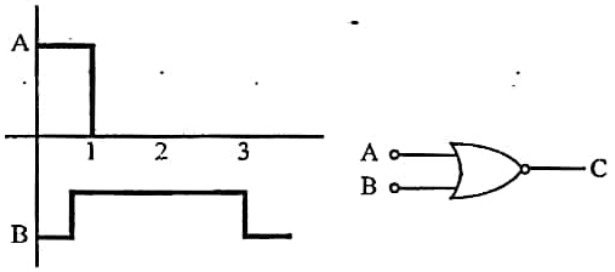
The truth table for the circuit can be written as

A	B	Z
0	0	
0	1	
1	0	
1	1	

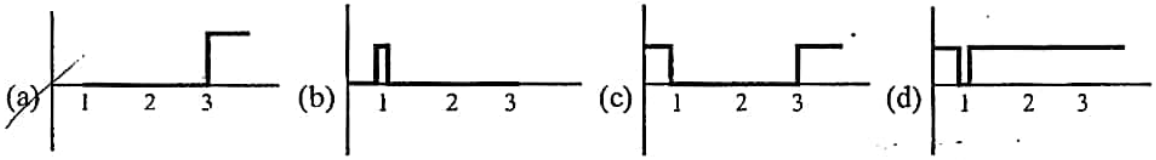
The entries in the Z column (vertically) are

(a) 1011 (b) 0100 (c) 1111 (d) 1010

68. The pulses shown as A and B are fed into the input of the gate shown below.



The output at C has the waveform



69. A J-K flip flop with J =1 and K=1 has a 10 kHz clock input. The Q output is

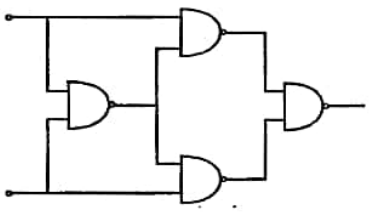
(a) a 10 kHz square wave (b) a 5 kHz square wave

(c) always LOW (d) always HIGH

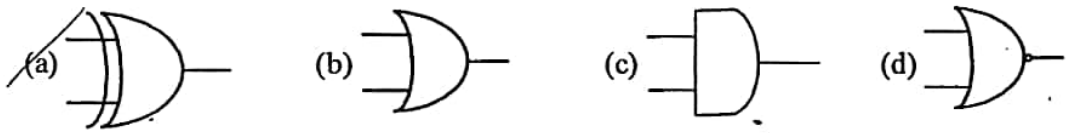
70. The binary number 1101 0100 0110 1111 can be written in hexadecimal as

(a) D467 (b) D46F (c) E46F (d) C46F

71. Consider the logic gate arrangement shown in the figure below



This arrangements is equivalent to the gate



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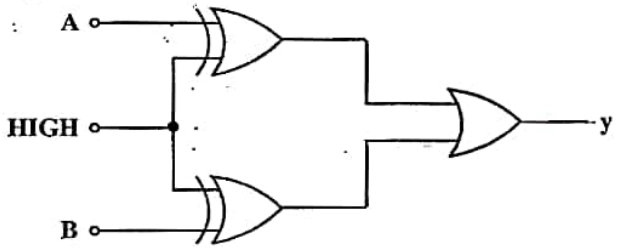
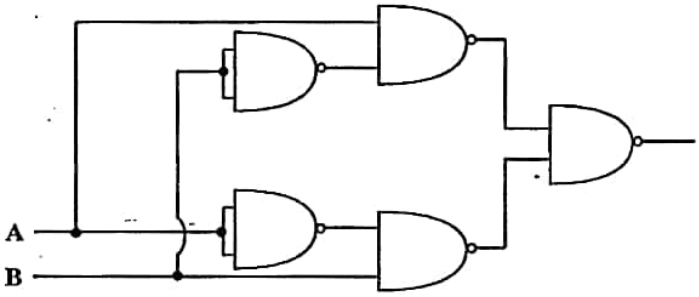
72. The logic circuit shown in the figure below.



implements the Boolean expression

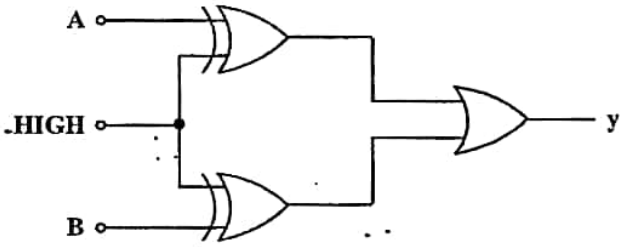
(a) $y = \overline{A.B}$ (b) $y = \bar{A}.\bar{B}$ (c) $y = A.B$ (d) $y = A + B$

73. The circuit shown below uses only NAND gates. Find the final output



(a) A XOR B (b) A AND B (c) A OR B (d) A NOR B.

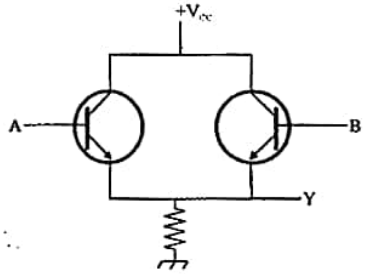
74. The logic circuit shown in the figure below.



implements the Boolean expression

(a) $y = \overline{A.B}$ (b) $y = \bar{A}.\bar{B}$ (c) $y = A.B$ (d) $y = A + B$

75. The circuit shown in the figure function as



(a) an OR gate (b) an AND gate (c) a NOR gate (d) a NAND gate

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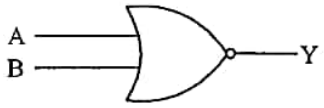
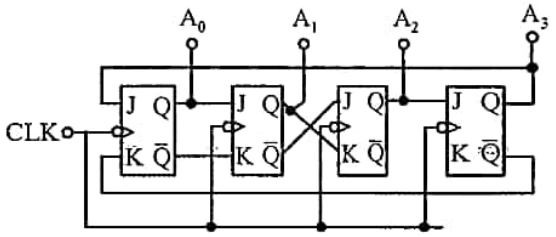
76. Consider the circuit shown below.



The minimum number of NAND gates required to design this circuit is

(a) 6 (b) 5 (c) 4 (d) 3

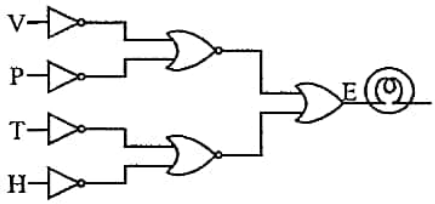
77. A counter consists of four fip-flops connected as shown in the figure.



If the counter is initialized as $A_0\ A_1\ A_2\ A_3 = 0110$, the state after the next clock pulse is

(a) 1000 (b) 0001 (c) 0011 (d) 1100

78. Four digital outputs V, P, T and H monitor the speed v, tyre pressure p, temperature t and relative humidity h of a car. These outputs switch from 0 to 1 when the values of the parameters exceed 85 km/hr, 2 bar, 40°C and 50%, respectively. A logic circuit that is used to switch ON a lamp at the output E is shown below.



Which of the following conditions will switch the lamp ON?

(a) $v < 85\text{km/hr}, p < 2\text{bar}, t > 40^\circ\text{C}, h > 50\%$

(b) $v < 85\text{km/hr}, p < 2\text{bar}, t > 40^\circ\text{C}, h < 50\%$

(c) $v > 85\text{km/hr}, p < 2\text{bar}, t > 40^\circ\text{C}, h < 50\%$

(d) $v > 85\text{km/hr}, p < 2\text{bar}, t < 40^\circ\text{C}, h > 50\%$

79. If one of the inputs of a J-K flip flop is high and the other is low, then the outputs Q and $\bar{Q}$

(a) oscillate between low and high in race-around condition

(b) toggle and the circuit acts like a T flip flop

(c) are opposite to the inputs

(d) follow the inputs and the circuit acts like an R-S flip flop

80. A 4-variable switching function is given by $f = \Sigma(5,7,8,10,13,15) + d(0,1,2)$, where d is the do-not-care-condition. The minimized form of f in sum of products (SOP) form is

(a) $\bar{A}\bar{C} + \bar{B}\bar{D}$ (b) $A\bar{B} + C\bar{D}$ (c) $AD + BC$ (d) $\bar{B}\bar{D} + BD$

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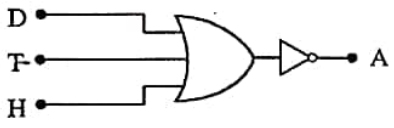
81: A control circuit needs to be designed to save on power consumption by an air-conditioning unit A in a windowless room with a single door. The room is fitted with the following devices:

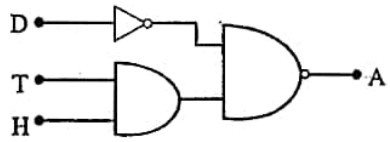
(1) A temperature sensor T, which is enabled (T = 1) whenever the temperature falls below a pre-set value;

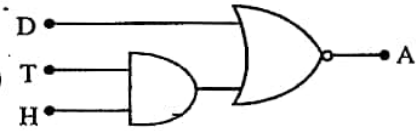
(2) A humidity sensor H, which is enabled (H = 1) whenever the humidity falls below a certain pre-set value;

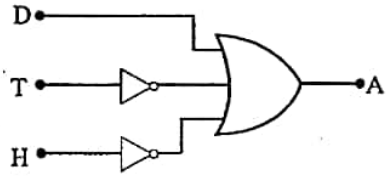
(3) A sensor D on the door, which is triggered (D = 1) whenever the door opens

Which of the following logical circuits will turn the air-conditioning unit off (A = 0) whenever the door is opened or when the both temperature and humidity are below their pre-set values?

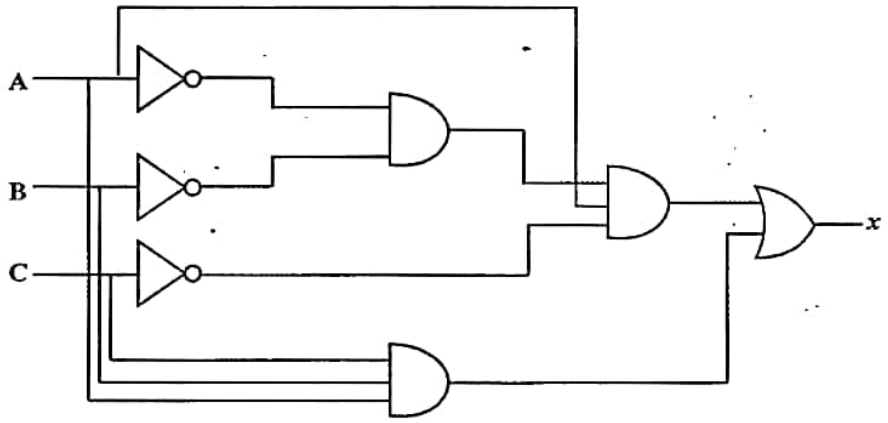
(a) 

(b) 

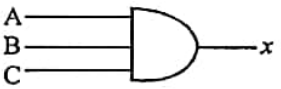
(c) 

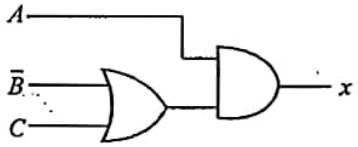
(d) 

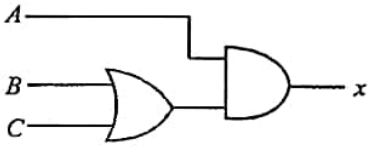
82. For the logic circuit shown in the figure below

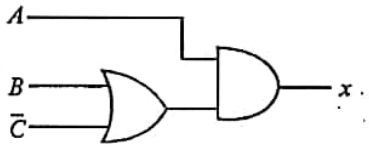


a simplified equivalent circuit is

(a) 

(b) 

(c) 

(d) 

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Answer Kye: NETWORKS

1. (a)	2. (c)	3. (d)	4. (c)	5. (a)	6. (a)	7. (d)
8. (a)	9. (b)	10. (d)	11. (b)	12. (d)	13. (b)	14. (d)
15. (b)	16. (d)	17. (c)	18. (a)	19. ( )	20. (a)	21. (c)
22. (b)	23. (b)	24. (a)	25. (b)	26. (a)	27. (a)	28. (b)
29. (b)	30. (b)	31. (a)	32. (a)	33. (b)	34. (a)	35. (b)
36. (a)	37. (d)	38. (a)	39. (c)	40. (b)	41. (b)	42. (d)
43. (c)	44. (a)	45. (a)	46. (d)	47. (b)	48. (b)	49. (a)
50. (b)	51. (c)	52. (b)	53. (a)	54. (a)	55. (b)	56. (c)
57. (a)	58. (a)	59. (d)	60. (c)	61. (b)	62. (d)	63. (a)
64. (b)	65. (d)	66. (b)	67. (c)	68. (b)	69. (a)	70. (a)
71. (b)	72. (d)	73. (a)	74. (b)	75. (b)	76. (a)	77. (c)
78. (b)	79. (c)	80. (c)	81. (d)	82. (b)	83. (c)	84. (b)
85. (b)	86. (a)	87. (b)	88. (1.25)	89. (b)	90. (d)	91. (c)
92. (a)	93. (c)	94. (a)	95. (3.15)	96. (c)	97. (b)	98. (a)
99. (c)	100. (1.4 to 1.7)		101. (9.99 to 10.01)		102. (b)	

Answer Kye: OP-AMP

1. (a)	2. (b)	3. (a)	4. (c)	5. (a)	6. (b)	7. (c)
8. (a)	9. (b)	10. (d)	11. (c)	12. (d)	13. (d)	14. (b)
15. (c)	16. (c)	17. (c)	18. (a)	19. (a)	20. (d)	21. (a)
22. (d)	23. (b)	24. (c)	25. (b)	26. (c)	27. (c)	28. (a)
29. (a)	30. (d)	31. (a)	32. (b)	33. (a)	34. (a)	35. (b)
36. (d)	37. (a)	38. (a)	39. (d)	40. (c)	41. (c)	42. (b)
43. (c)	44. (c)	45. (c)	46. (b)	47. (c)	48. (b)	49. (a)
50. (a)	51. (c)	52. (d)	53. (b)	54. (d)	55. (b)	56. (c)
57. (a)	58. (b)	59. (b)	60. (b)	61. (d)	62. (d)	63. (d)
64. (b)	65. (c)	66. (b)	67. (a)	68. (c)	69. (b)	70. (c)
71. (d)	72. (b)	73. (c)	74. (a)	75. (a)	76. (b)	77. (c)
78. (a)	79. (b)	80. (d)	81. (b)			

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Anwer Key: DIGITAL ELECTRONICS

1. (c)	2. (b)	3. (d)	4. (b)	5. (d)	6. (d)	7. (c)
8. (c)	9. (a)	10. (a)	11. (b)	12.(d)	13.(b)	14. (c)
15. (c)	16. (b)	17. (a)	18. (d)	19. (b)	20. (a)	21. (c)
22. (c)	23. (a)	24. (c)	25. (d)	26. (a)	27. (a)	28. (c)
29. (b)	30. (a)	31. (a)	32. (b)	33. (d)	34. (a)	35. (d)
36. (c)	37. (c)	38. (d)	39. (c)	40. (c)	41. (d)	42. (c)
43.(d)	44. (d)	45. (d)	46. (d)	47. (a)	48. (d)	49. (a)
50. (a)	51. (a)	52. (d)	53. (b)	54. (d)	55. (a)	56. (b)
57. (b)	58. (c)	59. (a)	60. (a)	61. (d)	62. (d)	63. (d)
64. (d)	65. (d)	66. (c)	67. (a)	68. (a)	69. (b)	70. (b)
71. (a)	72. (a)	73. (a)	74. (d)	75. (a)	76. (c)	77. (c)
78. (a)	79. (d)	80. (d)	81. (c)	82. (d)	83. (6.99 to 7.01)	

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